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GRL USB Type-C/PD Test Solution

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Type C Product trend

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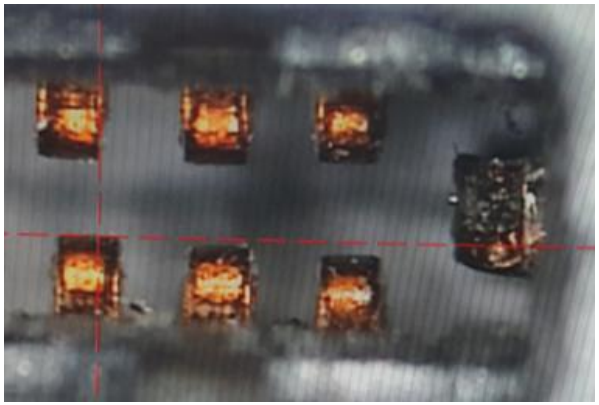
Interface



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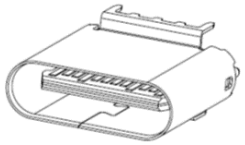
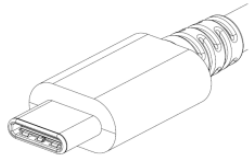
USB Type-C Full-Feature Receptacle



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

USB Type-C Full-Feature Plug



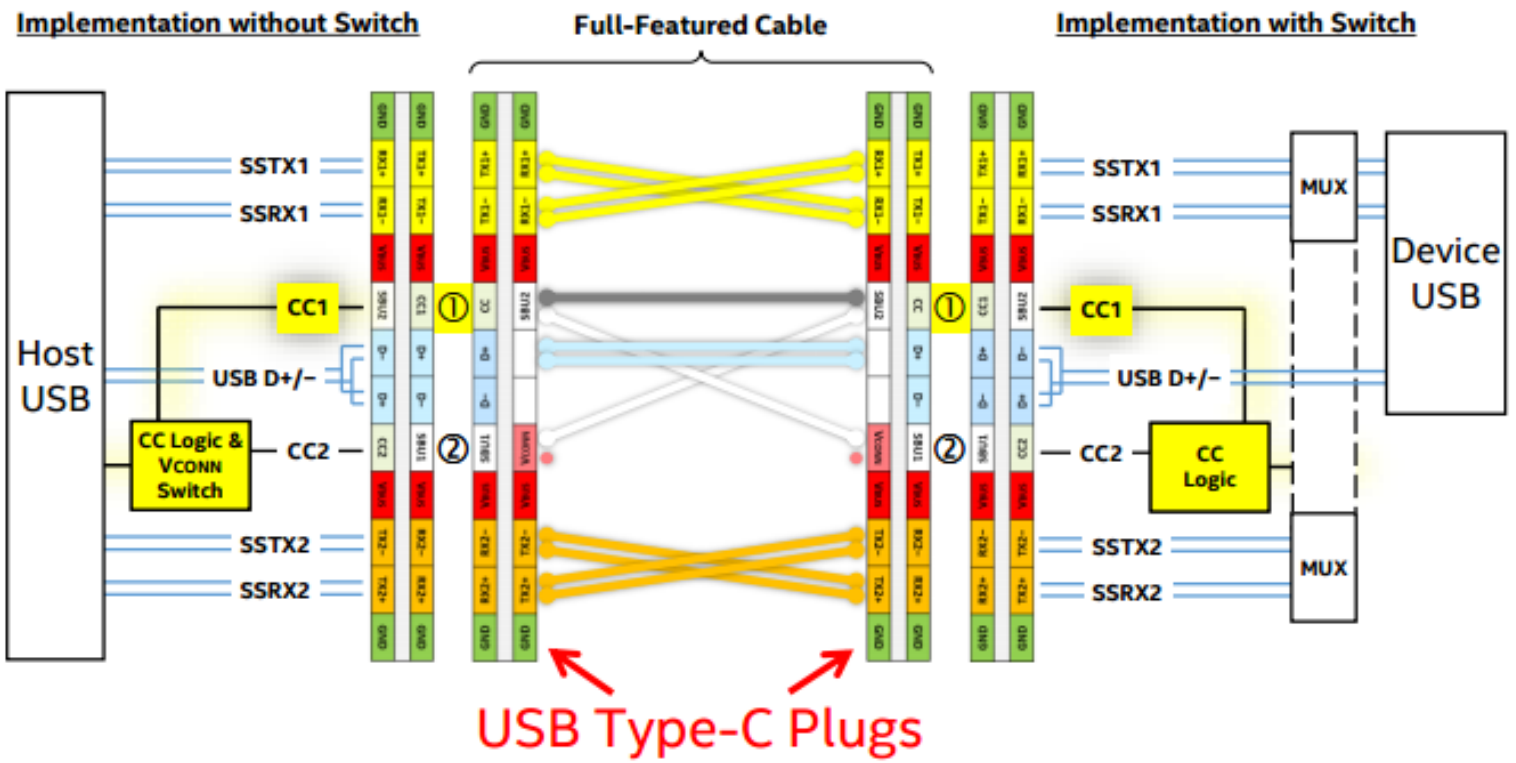
A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Understanding USB Type-C port behaviors

- Power roles:
  - Source – typical of Standard-A host or hub ports
  - Sink – typical of Standard-B or Micro-B device ports
  - Dual-Role Power – can be either a Source or a Sink
- Data roles:
  - Host-mode only – typical of Standard-A host or hub ports
  - Device-mode only – typical of Standard-B or Micro-B device ports
  - Dual-Role Data – typical of “on-the-go” ports

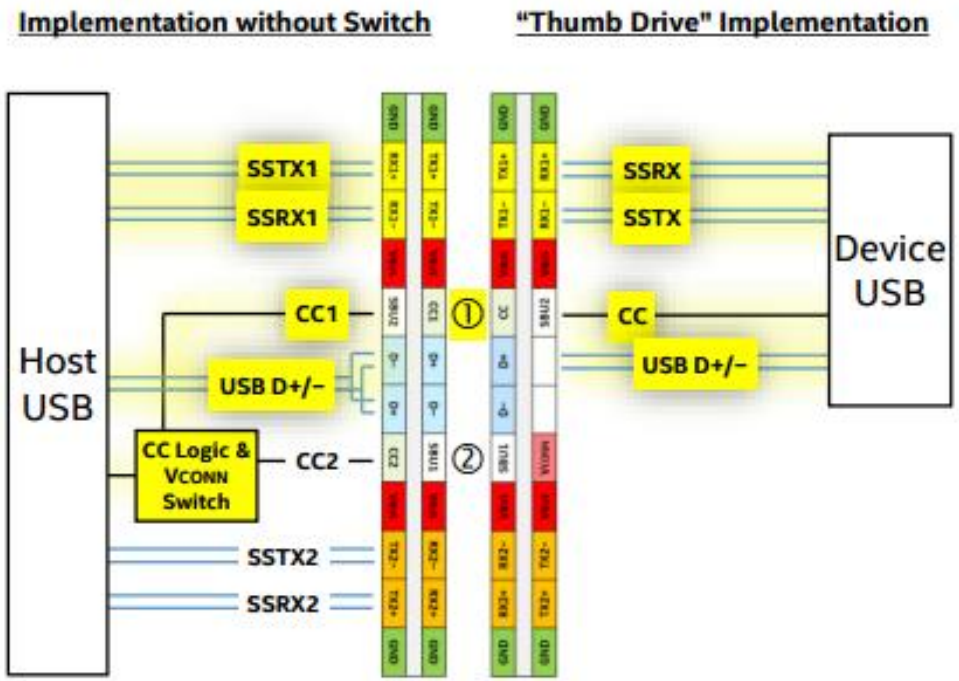
- Roles can be dynamically swapped using USB PD
  - Power role swap, data role swap

USB Type-C* Functional Model



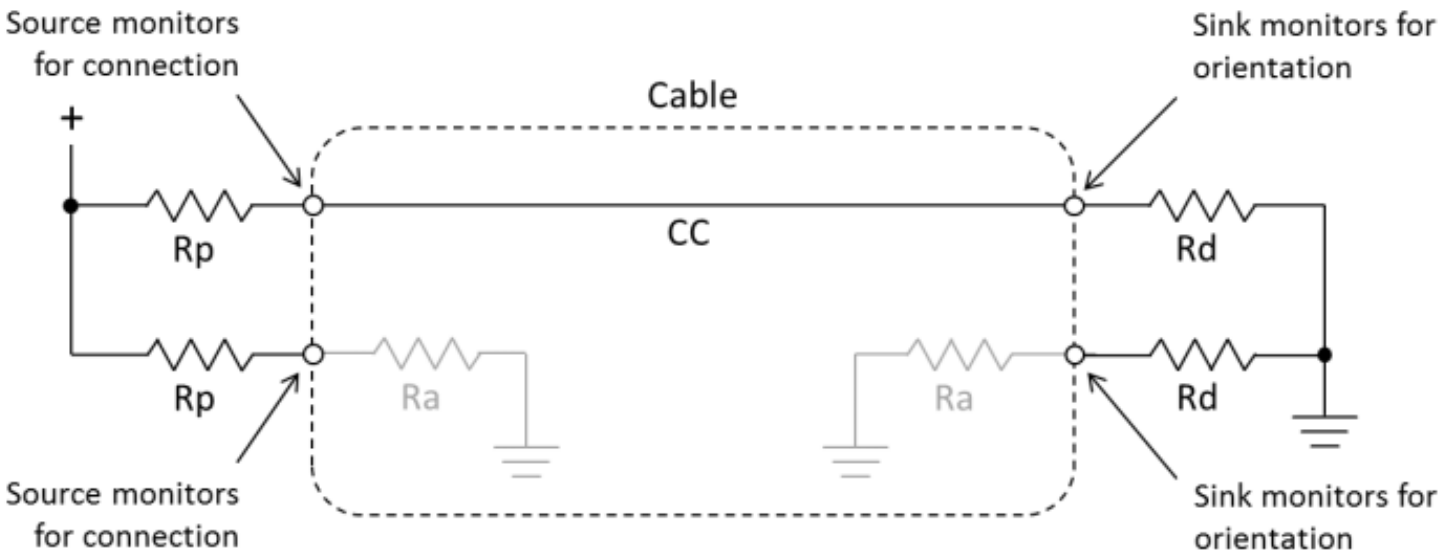
CC wire determines orientation through the cable

Direct Connect Functional Model



⇨ Un-flipped – Position ①

USB Type-C* – Pull-Up/Pull-Down CC Model



- Host side can substitute current sources for Rp
- Powered cables introduce Ra at the “unwired” CC pins which are used to indicate the need for VCONN over one of those pins

USB Type-C – Source (Host) Detected Connection States

	CC1	CC2	State	Position	
No device attached	Open	Open	Nothing attached	N/A	
	Rd	Open	Sink attached	①	*Most common states*
	Open	Rd		②	
	Open	Ra	Powered cable without Sink attached	①	
	Ra	Open		②	
Device attached	Rd	Ra	Powered cable with Sink or VCONN-powered Accessory attached	①	← Not flipped
	Ra	Rd		②	← Flipped
	Rd	Rd	Debug Accessory Mode attached (Appendix B)	N/A	
	Ra	Ra	Audio Adapter Accessory Mode attached (Appendix A)	N/A	

The CC pins *magic decoder ring* from the Source perspective

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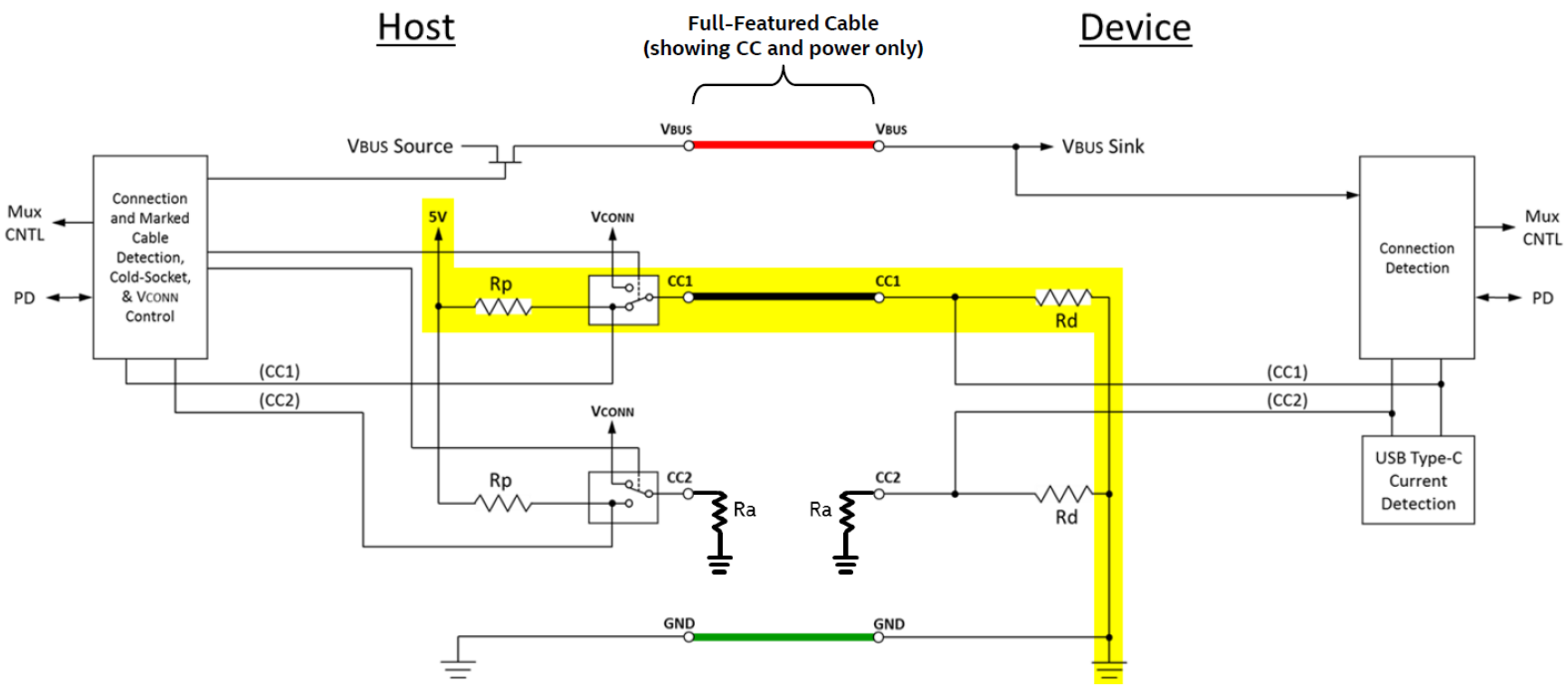
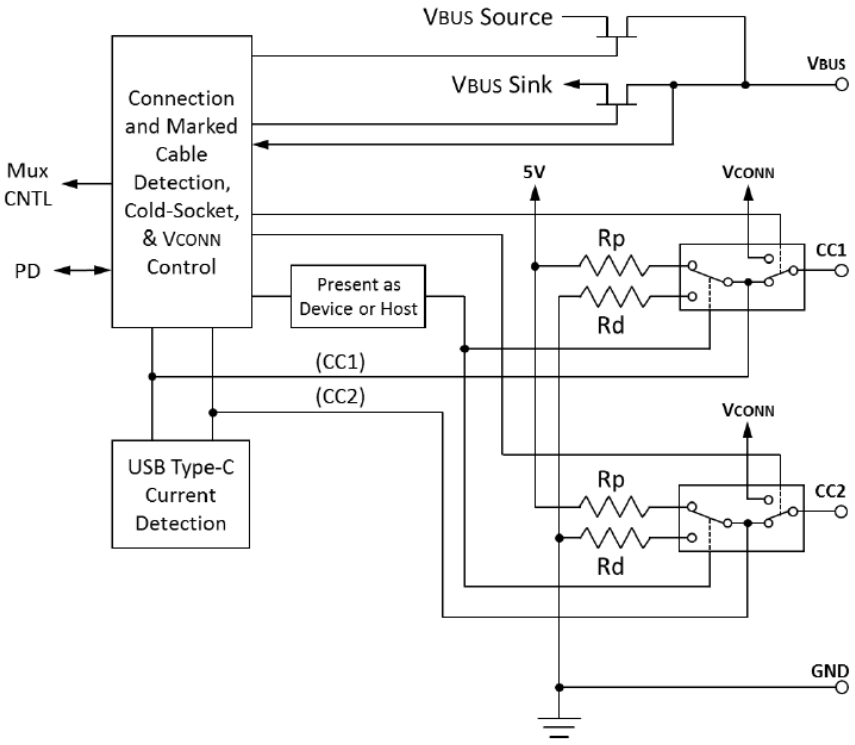
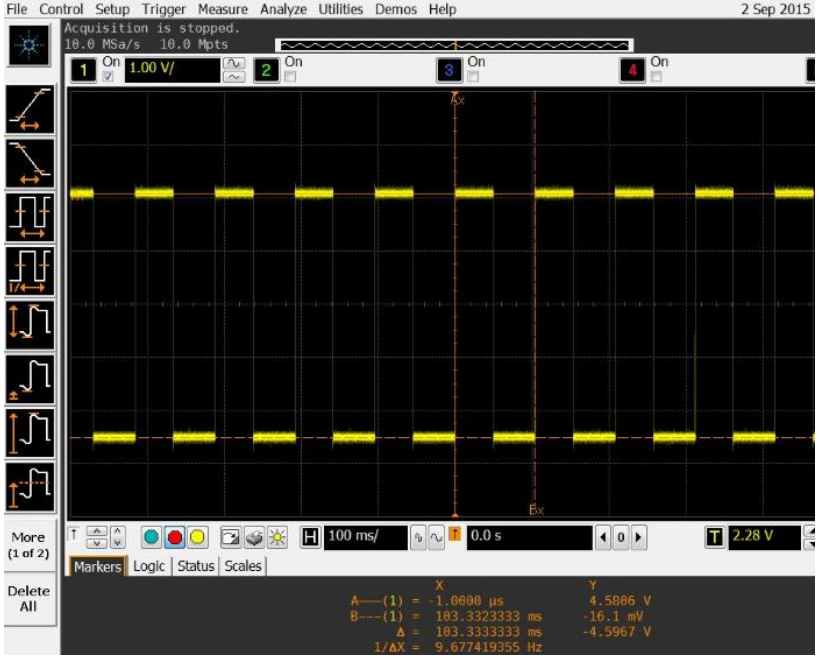
Basic Host Meets Basic Device



DRP – Product Capable of Either Host or Device



- DRP = Host + Device
  - Aligns to correct role based on whatever gets attached
- For discovery, toggles between presenting as a source (host) or sink (device)
  - Cycles 10 – 20 times per second



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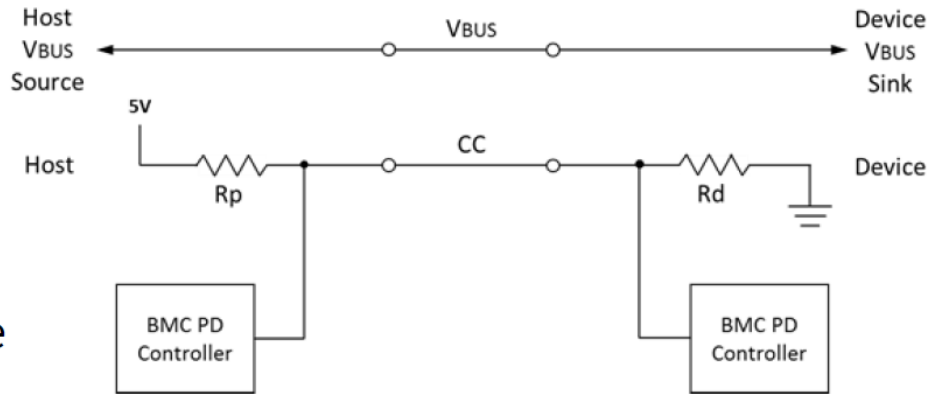
USB Type-C* – Power Options

- All solutions required to support Default USB Power appropriate to product – *as defined by USB 2.0 and USB 3.1*

- Extension options:
  - USB Type-C Current – Defines 1.5 A and 3 A @ 5 V ranges
  - USB BC 1.2 (also requires support of USB Type-C High Current)
  - USB Power Delivery (PD) – Variable voltage/current up to 5 A @ 20 V



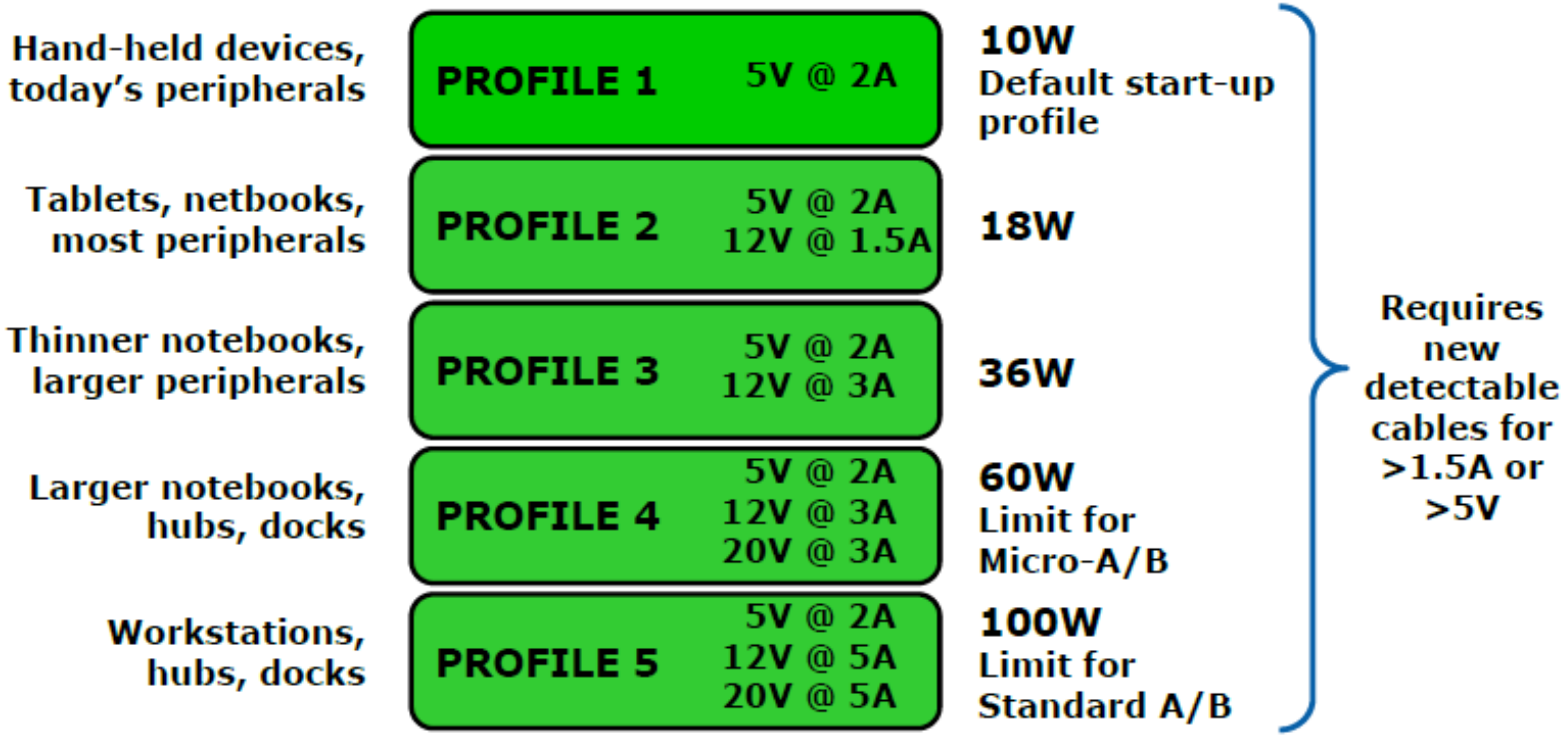
- USB PD for USB Type-C implementation is DC coupled and is based on Biphase Mark Coding (BMC) signal encoding over the CC wire

Table 4-13 DFP CC Termination (Rp) Requirements

DFP Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

USB Power Delivery Profiles

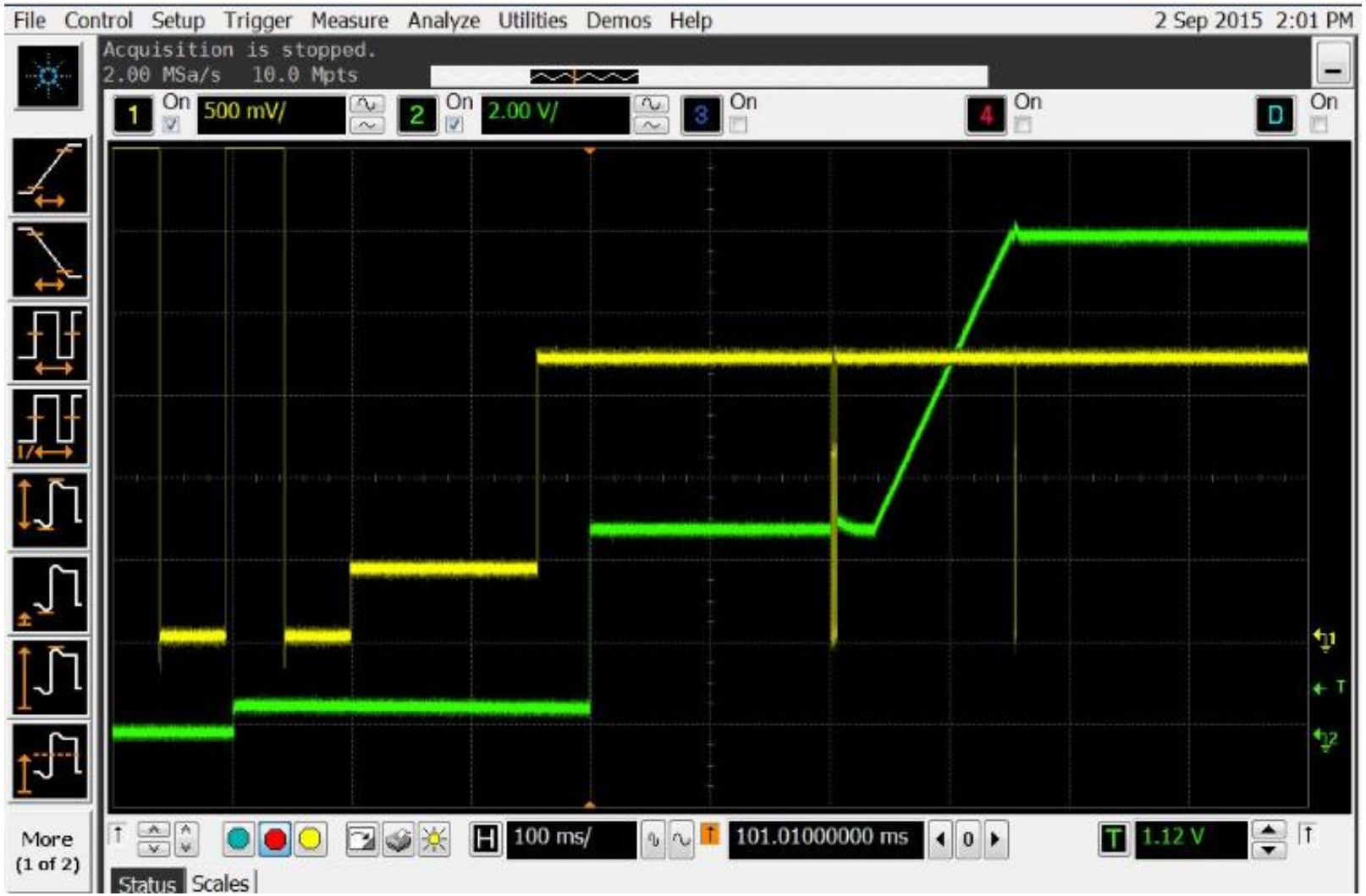
Source capabilities organized as profiles



- Source and Sink capabilities within a given product are not required to be the same

Ultimate goal: ship without in-box power adapter

- Eco-friendly goal: fewer discarded power bricks
- To meet this goal user has to be confident:
  - Power supply that was in-box with some other device will work well
  - They know what to order to get a second power adapter
- Chromebooks support Wattage based rules for user friendly adapters
  - (May change since rules are still being defined, today using 5/12/20V)
  - w <= 15W: provide 5V @ (w/5) A
  - 15W < w <= 27W: provide 5V @ 3A and 9V @ (w/9) A
  - 27W < w <= 45W: provide 5V @ 3A, 9V @ 3A, 15V @ (w/15) A
  - 45W < w < 100W: provide 5V @ 3A, 9V @ 3A, 15V @ 3A, 20V @ (w/20) A



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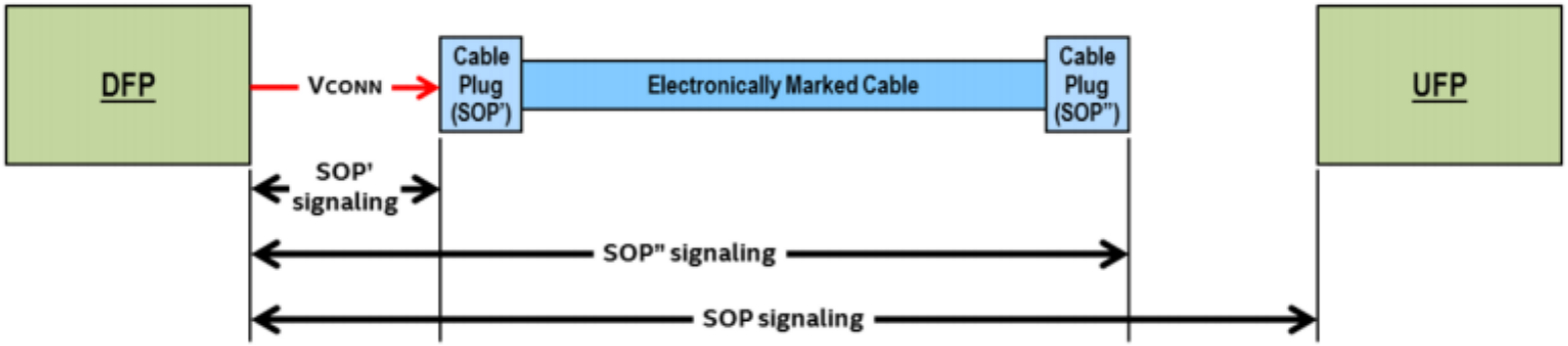
8	D…	Vendor Defined	SOP1-Syn…	Discover Identity-Initiator	Data	0	0x10 0x4F	0xFF008…	0xC704DD7B
9	DFP	Source Capabilities	SOP-Sync…	Fixed Supply;Variable Su…	Data	0	0x61 0x61	0x9903C…	0xC704DD7B
10	UFP	Good CRC	SOP-Sync…		Control	0	0x00 0x41		0xC704DD7B
11	UFP	Request	SOP-Sync…	Request;	Data	0	0x10 0x42	0x10025…	0xC704DD7B
12	DFP	Good CRC	SOP-Sync…		Control	0	0x01 0x61		0xC704DD7B
13	DFP	Accept	SOP-Sync…		Control	1	0x03 0x63		0xC704DD7B
14	UFP	Good CRC	SOP-Sync…		Control	1	0x02 0x41		0xC704DD7B
15	DFP	PS_RDY	SOP-Sync…		Control	2	0x05 0x66		0xC704DD7B
16	UFP	Good CRC	SOP-Sync…		Control	2	0x04 0x41		0xC704DD7B

Selected Packet Details

- Source Capabilities(Header = 0x61 0x61)
- PDO[1] = Fixed Supply-Source (0x96 0x90 0x21 0x08)
- PDO[2] = Variable Supply (non-battery)-Source (0x2C 0x91 0xC1 0x88)
- PDO[3] = Variable Supply (non-battery)-Source (0x2C 0x91 0x41 0x8B)
- PDO[4] = Variable Supply (non-battery)-Source (0x2C 0x31 0x02 0x8F)
- PDO[5] = Variable Supply (non-battery)-Source (0x2C 0xD1 0xC2 0x92)
- PDO[6] = Variable Supply (non-battery)-Source (0x2C 0xC1 0x03 0x99)

Bit(s)	Field Description	Raw Data	Value
B31..30	Variable Supply (non-batte…	0x2	Variable Supply (non-battery)
B29..20	Maximum Voltage	0x190	20000mV
B19..10	Minimum Voltage	0xF0	12000mV
B9..0	Maximum Current	0x12C	3000mA

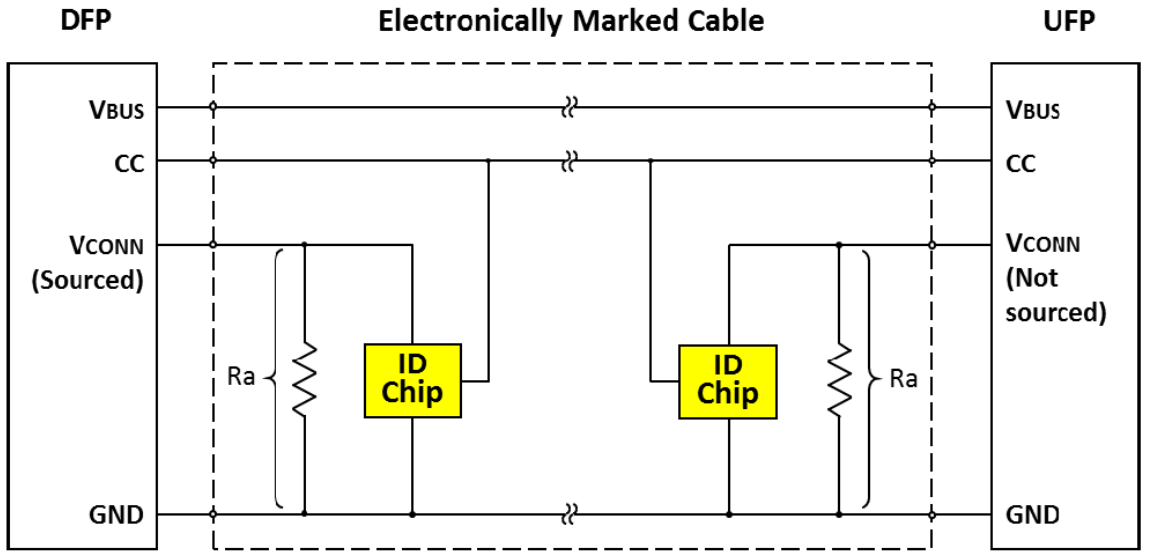
Communicating With Cables



- Original port-to-port architecture expanded
  - Cable identification
  - Manage active cables
- How was multi-drop added?
  - Packet structure unchanged
  - Start of packet is message 'address' (SOP'/SOP")
- Single initiator of multi-drop message sequences
  - Source can initiate communication SOP' prior to an explicit contract
  - Within an explicit contract only DFP can initiate communication SOP'/SOP"
- Cable Plug or UFP are never allowed to initiate messages

Electronically Marked Cables

- All USB 3.1 Type-C* cables require electronic marking
  - Also required for USB 2.0 Type-C cables with a current rating over 3 A



- Electronic marking mechanism (SOP') defined in USB Power Delivery 2.0

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length	Current Rating	Power Delivery	Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3A	Supported	Optional
CC2-5					5A		Required
CC3G1-3	C	C	USB 3.1 Gen 1	≤ 2 m	3A	Supported	Required
CC3G1-5					5A		
CC3G2-3	C	C	USB 3.1 Gen 2	≤ 1 m	3A	Supported	Required
CC3G5-3					5A		

eMark VDM content

Selected Packet Details

Vendor Defined(Header = 0x51 0x4F)

PDO[1] = VDM-Header-Discover Identity-Responder ACK (0x41 0x80 0x00 0xFF)

PDO[2] = VDM-ID Header- (0x34 0x83 0x00 0x18)

Bit(s)	Field Description	Raw Data	Value
B31	Data Capable as USB Host	0x0	
B30	Data Capable as a USB Device	0x0	
B29..27	Product Type	0x3	Passive Cable
B26	Modal Operation Supported	0x0	
B25..15	Reserved	0x0	
B15..0	USB Vendor ID	0x8334	Unknown Vendor ID (33588)

PDO[3] = VDM-Cert Stat VDO- (0x00 0x00 0x00 0x00)

Bit(s)	Field Description	Raw Data	Value
B31..20	Reserved	0x0	
B19..0	Test ID	0x0	0

PDO[4] = VDM-Product VDO- (0x00 0x00 0x00 0x00)

Bit(s)	Field Description	Raw Data	Value
B31..20	USB Product ID	0x0	0
B19..0	bcdDevice	0x0	0

PDO[5] = VDM-Type Specific- (0xD2 0x2F 0x08 0x11)

Bit(s)	Field Description	Raw Data	Value
B31..28	Cable HW Version	0x1	1
B27..24	Cable Firmware Version	0x1	1
B23..20	Reserved	0x0	
B19..18	Cable Type	0x2	Type-C
B17	Type C	0x0	Plug
B16..13	Cable Latency	0x1	<10ns (~1m)
B12..11	Cable Termination Type	0x1	Both ends Passive, VCONN required
B10	SSTX1 Directionality Support	0x1	Configurable
B9	SSTX2 Directionality Support	0x1	Configurable
B8	SSRX1 Directionality Support	0x1	Configurable
B7	SSRX2 Directionality Support	0x1	Configurable
B6..5	VBUS Current Handling Capability	0x2	5A
B4	VBUS through cable	0x1	Yes
B3	SOP controller present?	0x0	SOP controller not present
B2..0	USB Superspeed Signaling Support	0x2	[USB3.1] Gen1 and Gen2

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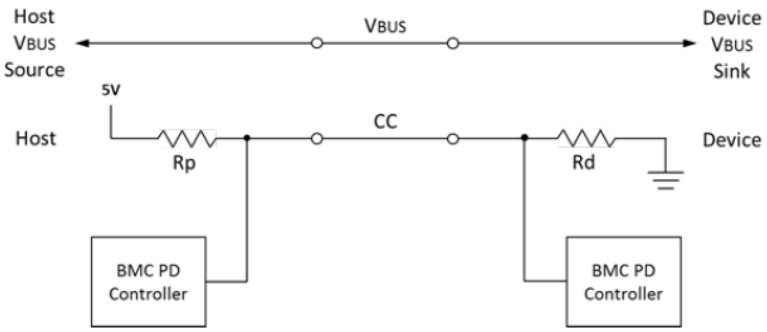
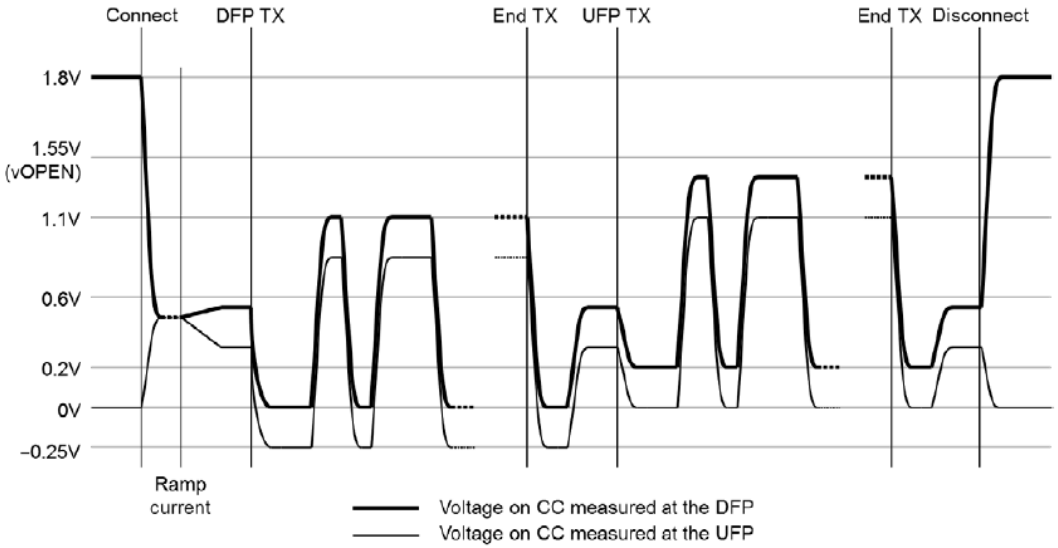
USB Power Delivery (PD) on USB Type-C

- USB PD 2.0 specifies DC-coupled Biphase Mark Coding (BMC) signal encoding for use over CC





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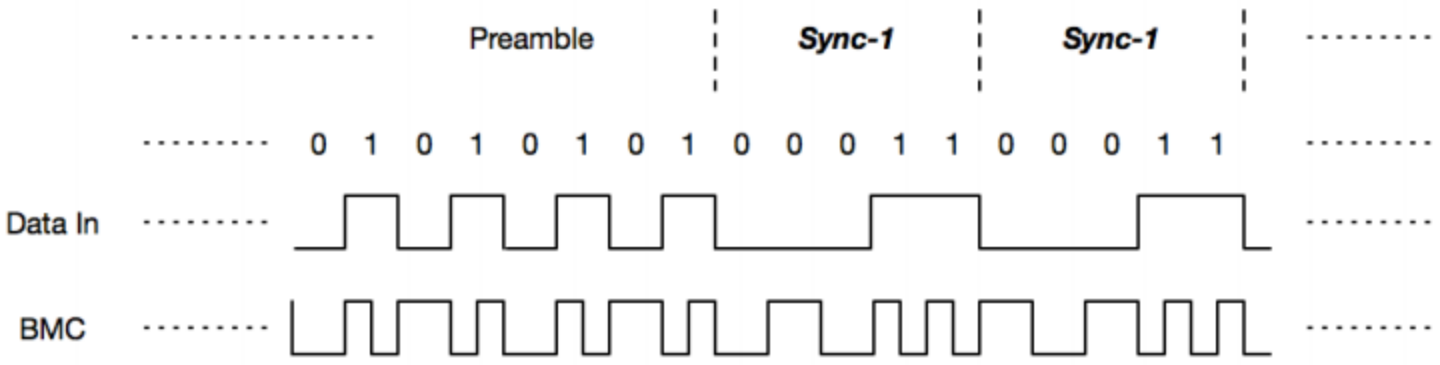
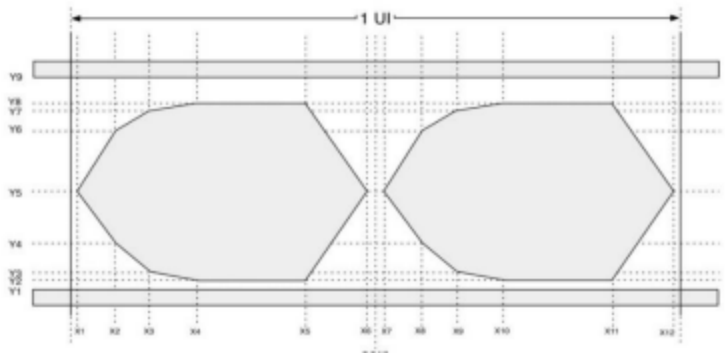
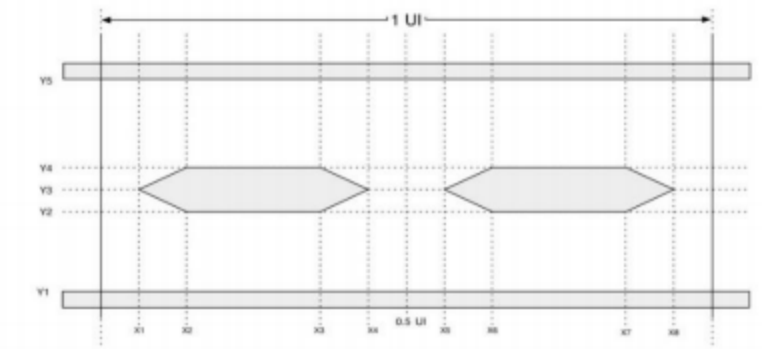
BMC Characteristics

- Biphase Manchester Coding
- 2 transitions for one and 1 transition for zero



- Defined by transmit and receive masks



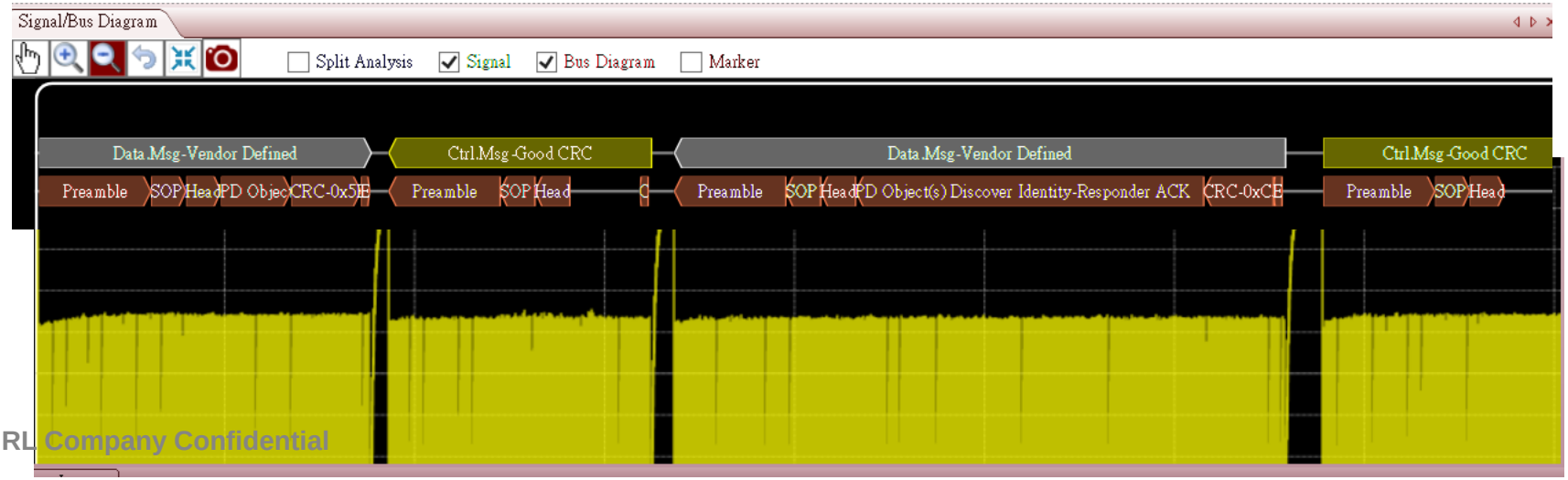


PD Packet Structure

Preamble(training for receiver)	SOP (Start Of Packet)	Header	Byte 0	Byte 1	•••

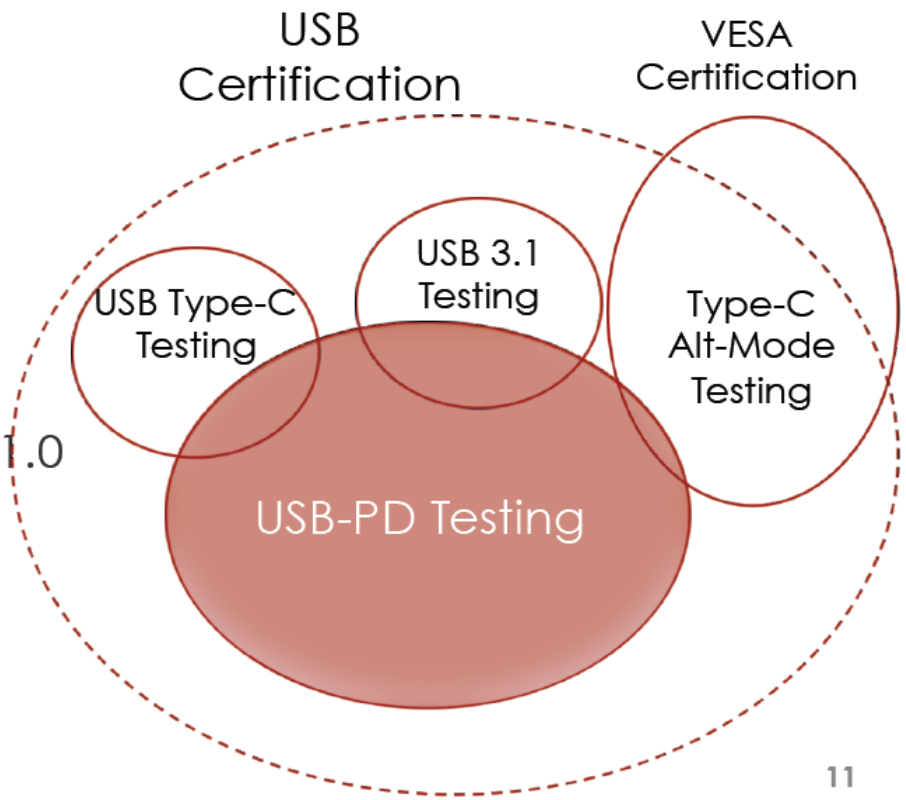
•••	Byte n-1	Byte n	CRC	EOP (End Of Packet)

- Packets preamble – allows receiver to synch up with transmitter
- SOP – Start of Packet – unique identifier
- PD Header – identifies type of packet and amount of data
- CRC – Error Checking
- EOP – End of Packet – unique identifier



USB-PD & DisplayPort Specification & CTS Overlap

- USB Power Delivery Rev2.0, V1.0
  - Chapter 2 - Overview Section including SOP* Comm and UFP/DFP Communications
  - Chapter 3 Type-A and TypeB Cable Assemblies & Connectors
  - Chaper 4 Electrical Requirements
  - Chapter 5 Physical Layer (BMC & FSK)
  - Chapter 6 Protocol Layer
  - Chapter 7 Power Supply
  - Chapter 8 Device Policy
  - Chapter 9 System Policy
- USB Type-C Cable Specification Rev1.0
  - Chapter 4 – Type-C Functional Testing
- DisplayPort Alt Mode on USB Type-C
  - Chapter 5 – Discovery and USB-PD



USB Power Delivery (XID) replace (EID)

USB-IF: USB Power Delivery XID Request Form

USB-IF Member companies requesting an XID range must complete the USB Power Delivery XID Request Form and submit to admin@usb.org

1. USB-IF Member companies are eligible to request XIDs from the USB-IF.
2. XIDs can be provided in blocks of 50.
    a. Note: Companies must first use their allotted XID block before requesting additional XIDs.
3. Please complete and email this form to admin@usb.org to request XIDs.
4. Once approved, USB-IF Administration will provide the block of XIDs. Please note that XIDs may only be used once.

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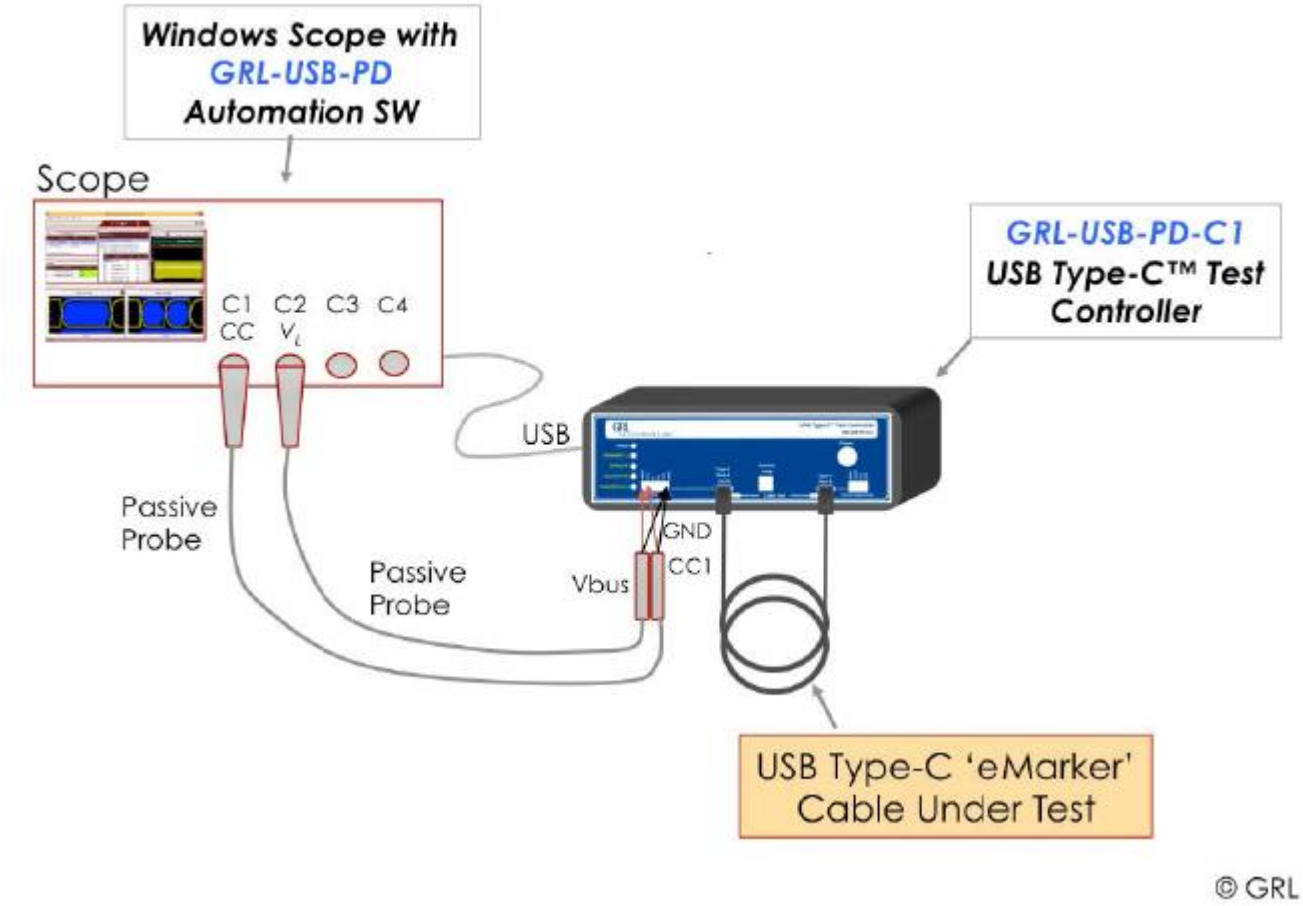
Confirm Test Setup (eMark Cable Example)



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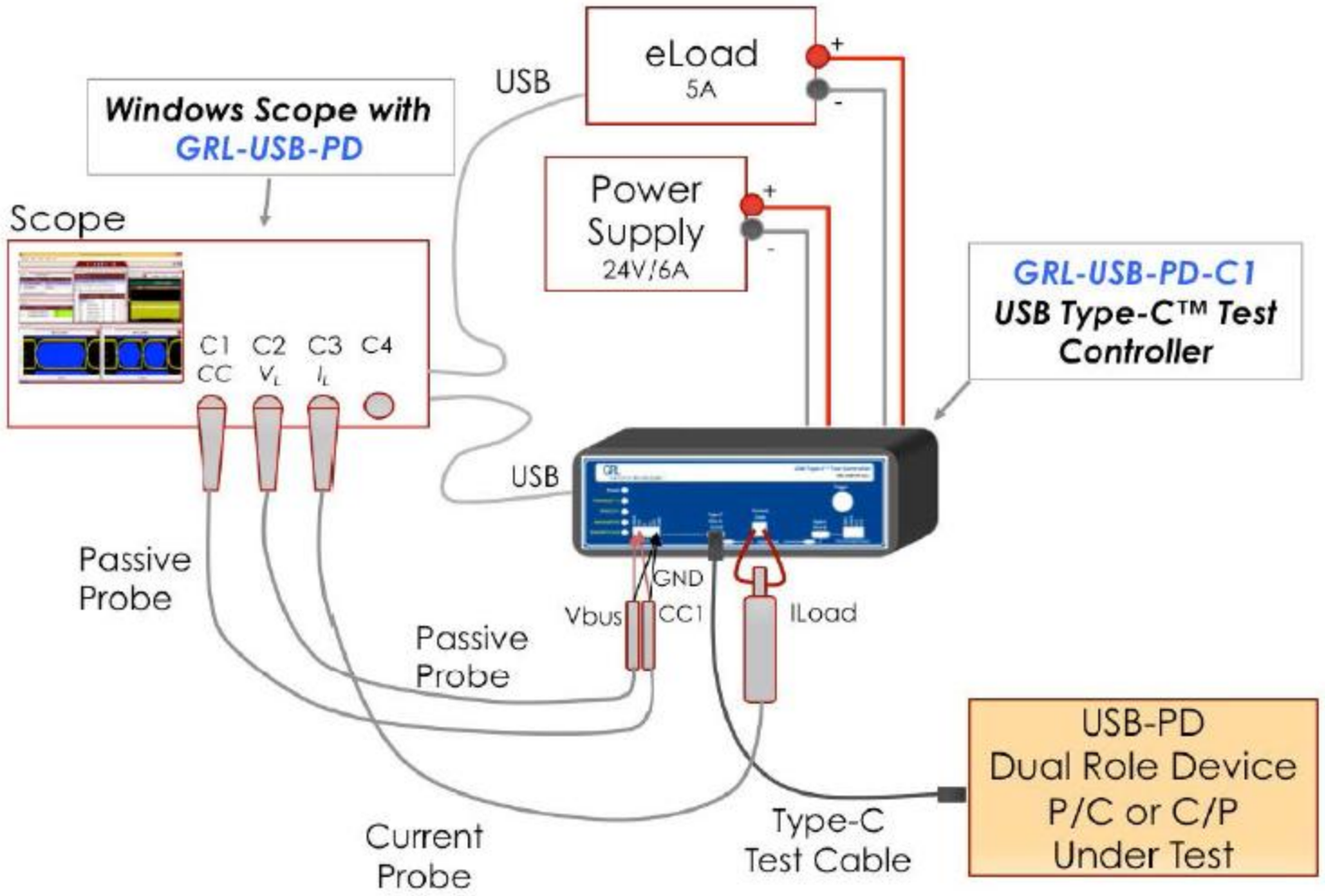
Confirm Test Setup (Provider/Consumer Example)



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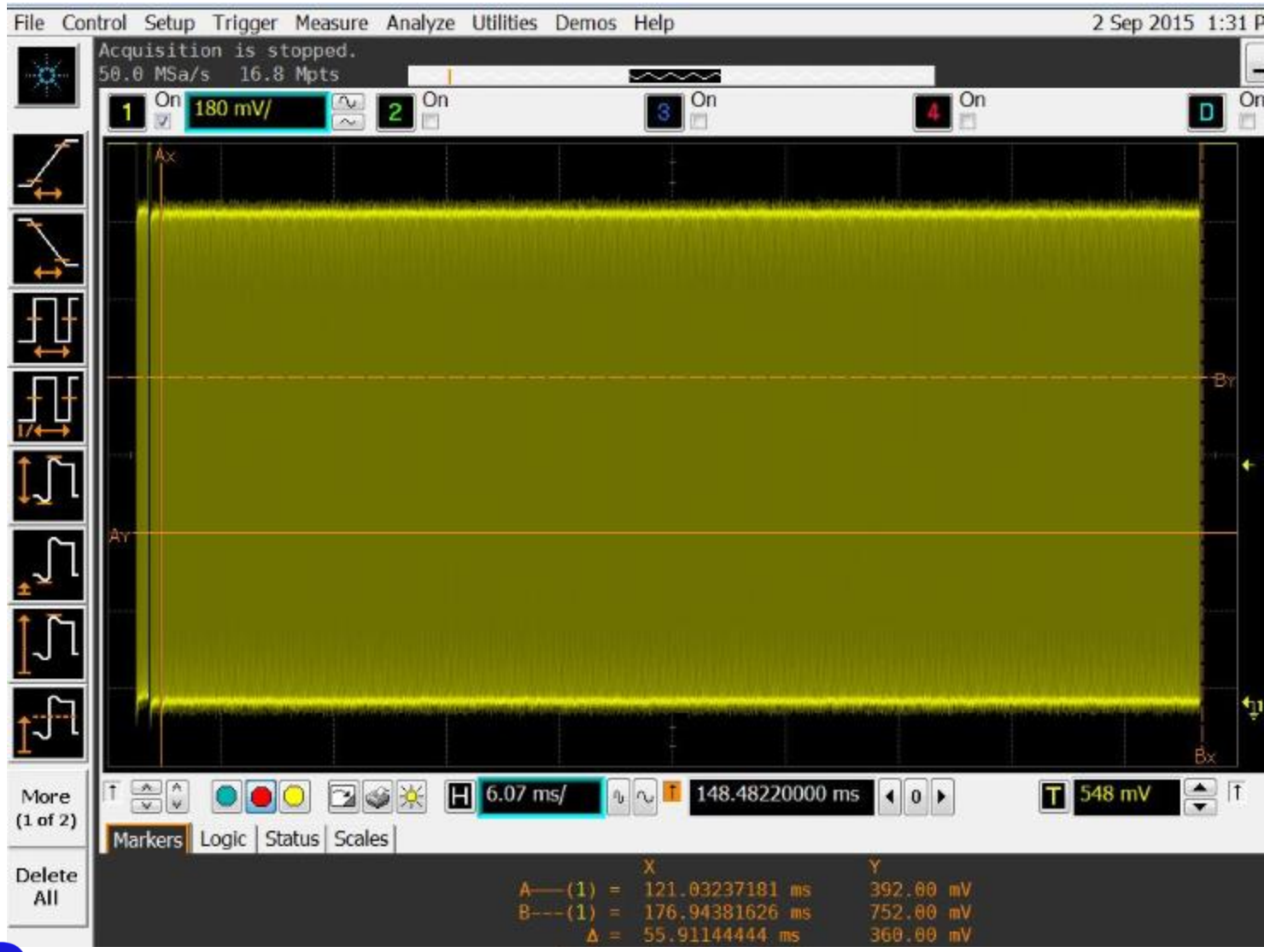
BIST Mode pattern (30ms-60ms)



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Test Coverage for Providers & Consumers (BMC-PHY)

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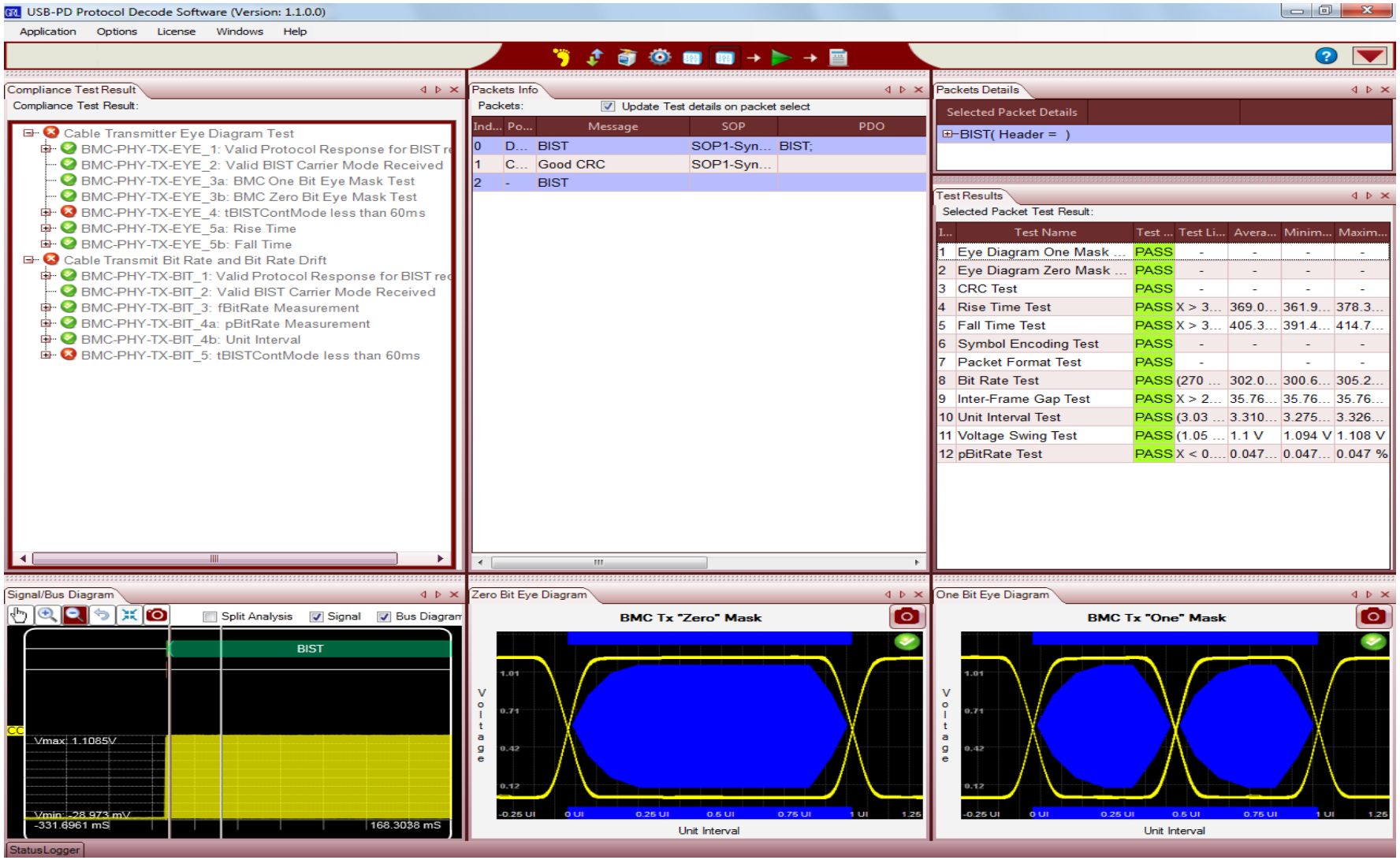

Ellisys DFP Protocol test

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USB PD Type-C Tests

- TD.PD.C.E1 DFP Attach/Detach Detection

USB PD Type-C Connection Tests

- TD.4.1 Initial Voltage
- TD.4.2 Source Connect Sink
- TD.4.3 Source Connect Sink Accessory
- TD.4.4 Source Connect DRP
- TD.4.5 Source Connect Audio Accessory
- TD.4.7 Source Connect Powered Accessory

USB PD Physical Tests

- TD.PD.PHY.E1 BIST Test Data
- TD.PD.PHY.E2 BIST Receiver Mode
- TD.PD.PHY.E3 BIST Transmitter Mode
- TD.PD.PHY.E4 Transmitter Bit Rate Drift
- TD.PD.PHY.E5 Transmitter Collision Avoidance
- TD.PD.PHY.E6 Receiver Swing Tolerance
- TD.PD.PHY.E7 Receiver Bit Rate Tolerance
- TD.PD.PHY.E8 Receiver Bit Rate Deviation Tolerance
- TD.PD.PHY.E9 Valid SOP Framing
- TD.PD.PHY.E10 Invalid SOP Framing
- TD.PD.PHY.E11 Valid SOP' Framing
- TD.PD.PHY.E12 Invalid SOP' Framing
- TD.PD.PHY.E13 Valid SOP" Framing
- TD.PD.PHY.E14 Invalid SOP" Framing
- TD.PD.PHY.E15 Valid SOP'/" Debug Framings
- TD.PD.PHY.E16 Valid Hard Reset Framing
- TD.PD.PHY.E17 Invalid Hard Reset Framing
- TD.PD.PHY.E18 Valid Cable Reset Framing
- TD.PD.PHY.E19 Invalid Cable Reset Framing
- TD.PD.PHY.E20 EOP Framing
- TD.PD.PHY.E21 Preamble

USB PD Link Tests

- TD.PD.LL.E2 Retransmission
- TD.PD.LL.E3 Soft Reset Usage
- TD.PD.LL.E4 Hard Reset Usage
- TD.PD.LL.E5 Soft Reset

- USB PD VDM Tests for UFPs and Cables
- USB PD DisplayPort Tests for UFPs and Cables

USB PD DisplayPort Tests for DFPs

- TD.PD.DPD.E1 DP SVID in Arbitrary Location
- TD.PD.DPD.E3 No Response to Enter Mode
- TD.PD.DPD.E4 Enter Mode Failed

USB PD Consistency Tests for UFPs and Cables

- TD.PD.VNDIU.E4 SOP* Handling
- TD.PD.VNDIU.E5 Source Capabilities
- TD.PD.VNDIU.E7 Accepts PR_Swap as Source
- TD.PD.VNDIU.E9 Requests PR_Swap as Source

Ellisys emark cable Protocol test

USB PD Type-C Tests

- TD.PD.C.E3 Cable Ra

» USB PD Type-C Connection Tests

USB PD Physical Tests

- TD.PD.PHY.E1 BIST Test Data
- TD.PD.PHY.E2 BIST Receiver Mode
- TD.PD.PHY.E3 BIST Transmitter Mode
- TD.PD.PHY.E4 Transmitter Bit Rate Drift
- TD.PD.PHY.E5 Transmitter Collision Avoidance
- TD.PD.PHY.E6 Receiver Swing Tolerance
- TD.PD.PHY.E7 Receiver Bit Rate Tolerance
- TD.PD.PHY.E8 Receiver Bit Rate Deviation Tolerance
- TD.PD.PHY.E9 Valid SOP Framing
- TD.PD.PHY.E10 Invalid SOP Framing
- TD.PD.PHY.E11 Valid SOP' Framing
- TD.PD.PHY.E12 Invalid SOP' Framing
- TD.PD.PHY.E13 Valid SOP" Framing
- TD.PD.PHY.E14 Invalid SOP" Framing
- TD.PD.PHY.E15 Valid SOP'/" Debug Framings
- TD.PD.PHY.E16 Valid Hard Reset Framing
- TD.PD.PHY.E17 Invalid Hard Reset Framing
- TD.PD.PHY.E18 Valid Cable Reset Framing
- TD.PD.PHY.E19 Invalid Cable Reset Framing
- TD.PD.PHY.E20 EOP Framing
- TD.PD.PHY.E21 Preamble

» USB PD Link Tests

USB PD VDM Tests for UFPs and Cables

- TD.PD.VDMU.E1 Discover Identity Response
- TD.PD.VDMU.E2 Discover SVIDs Response
- TD.PD.VDMU.E3 Discover Modes Response
- TD.PD.VDMU.E4 Enter Mode Response
- TD.PD.VDMU.E5 Exit Mode Response
- TD.PD.VDMU.E6 Discover Identity Response Time
- TD.PD.VDMU.E7 Discover SVIDs Response Time
- TD.PD.VDMU.E8 Discover Modes Response Time
- TD.PD.VDMU.E9 Enter/Exit Mode Response Time
- TD.PD.VDMU.E10 Discover Identity Wrong SVID
- TD.PD.VDMU.E11 Discover SVIDs Wrong SVID
- TD.PD.VDMU.E12 Discover Modes Wrong SVID
- TD.PD.VDMU.E13 Enter Mode Wrong SVID
- TD.PD.VDMU.E14 Exit Mode Wrong SVID
- TD.PD.VDMU.E15 Applicability
- TD.PD.VDMU.E17 Interruption by VDM Command

» USB PD DisplayPort Tests for UFPs and Cables

» USB PD DisplayPort Tests for DFPs

USB PD Consistency Tests for UFPs and Cables

- TD.PD.VNDIU.E1 VDM Identity
- TD.PD.VNDIU.E2 VDM SVIDs
- TD.PD.VNDIU.E3 VDM Modes
- TD.PD.VNDIU.E4 SOP* Handling
- TD.PD.VNDIU.E11 DisplayPort Alt-Modes

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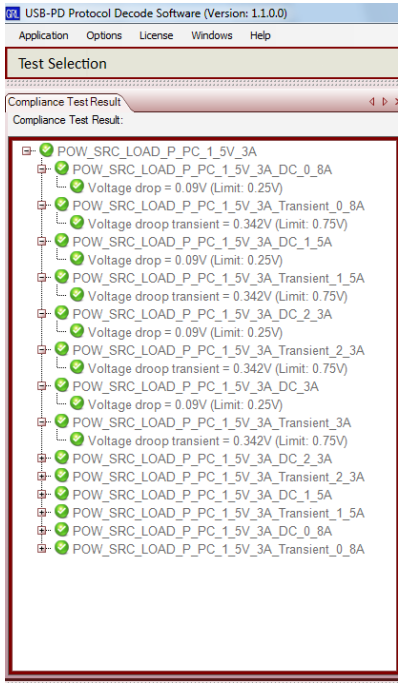
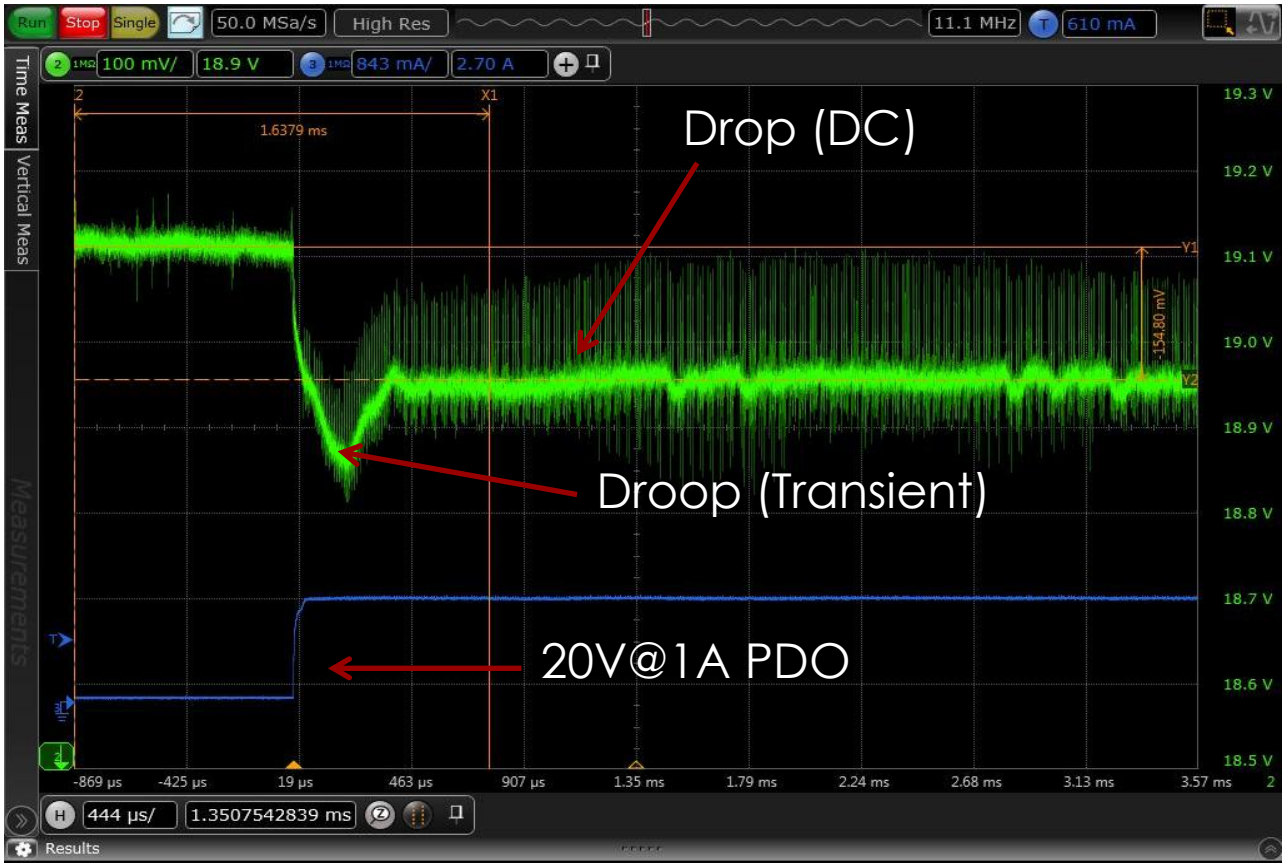
USB-PD Power Provider Compliance Tests

The Source output voltage shall be measured at the connector receptacle. The stability of the Source shall be tested in 1 25% load step increments from minimum load to maximum load and also from maximum load to minimum load.

BMC-POW-SRC-LOAD-P-PC: Source Dynamic Load Test, Provider or Provider/Consumer	Fail
BMC-POW-SRC-LOAD-P-PC_1	Fail
BMC-POW-SRC-LOAD-P-PC_2	Pass
PDO1:BMC-POW-SRC-LOAD-P-PC_3	Fail
PDO1:BMC-POW-SRC-LOAD-P-PC_4	Pass
PDO1:BMC-POW-SRC-LOAD-P-PC_5	Fail
PDO1:BMC-POW-SRC-LOAD-P-PC_6	Fail
Load 25%	Pass
Load 50%	Fail
Load 75%	Fail
Load 100%	Pass
Load 75%	Pass
Load 50%	Pass
Load 25%	Pass

Vbus 'Drop' and 'Droop' Compliance Measurements Made on eLoad Transition





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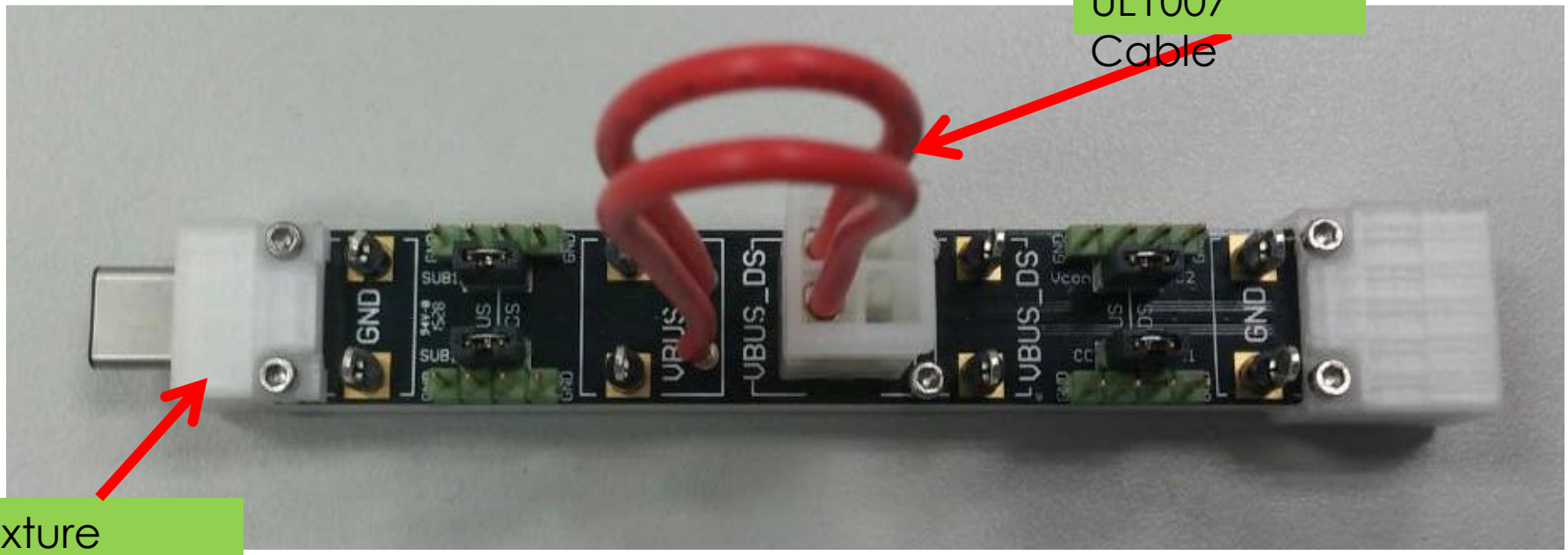
USB PD Fixture



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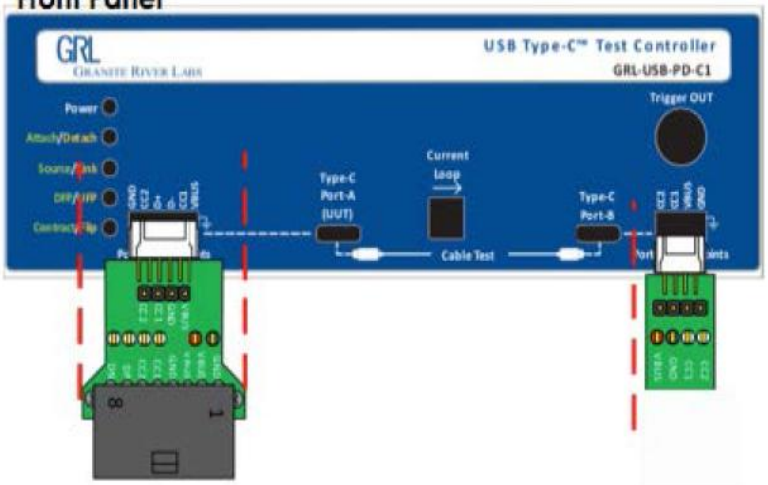
Rear Panel

Front Panel



Flexible USB Type-C Test Controller

GRL-USB-PD-C1 is a flexible test controller designed for USB-PD Compliance testing and more.

Rear Panel:

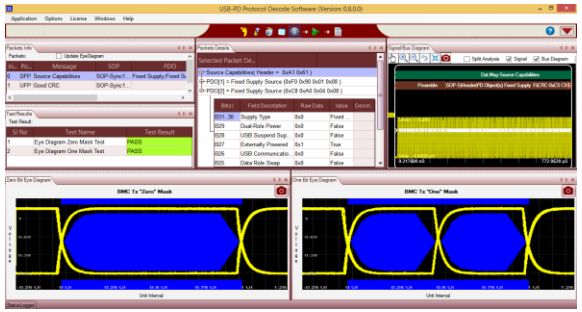
- E-Load - Connects to external Electronic load for load testing of the Unit Under Test (UUT)
- Power – Provides options to Power controller and UUT
- USB Control - USB 3.0 Control Connection to Windows based Oscilloscope
- Type-C SBU – Input of SBU Signal. Output appears on Type-C Port A Connector
- System - External connection to upgrade FPGA Firmware

Front Panel:

- Indicator LEDs – Power, Attach/Detach, Source/Sink, DFP/UFP, Contract/Flip
- Type-C Port-A (UUT) – Primary Type-C Connection for Unit Under Test (UUT)
- Port-A Probe Points – Probe Port-A (Gnd, CC1, D+/D-, CC2, and Vbus) with external adapter. Including interface connectors for High Speed test fixtures
- Type-C Port-B – Secondary Type-C Connection for Cable Testing
- Port-B Probe Points – Probe Port-B (Gnd, CC1, CC2, Vbus) with external adapter
- Trigger Out – Event trigger for Oscilloscope

GRL Type-C/USB-PD Electrical & Protocol Test Software (GRL-USB-PD)

- **Rev 1.0 - SW Available Today (GRL-USB-PD)**
- Supports multiple Vendors Scopes and Performance Levels
  - BMC Eye Diagram & Timing Measurements
    - BitRate, Risetime, CRC Check
  - Bus Diagram and Signal View Window
  - CC Line Packet Decode
  - Report Generator
  - VDM Decode for Cables and Adaptors



- **Rev 1.2 – with Controller Solution - Available Q4 2015**
  - Vbus (Voltage & Current) and Power Measurements
  - USB-PD Power Measurements
  - Automated Test Plan Creation based on USB Type-C Product Capabilities

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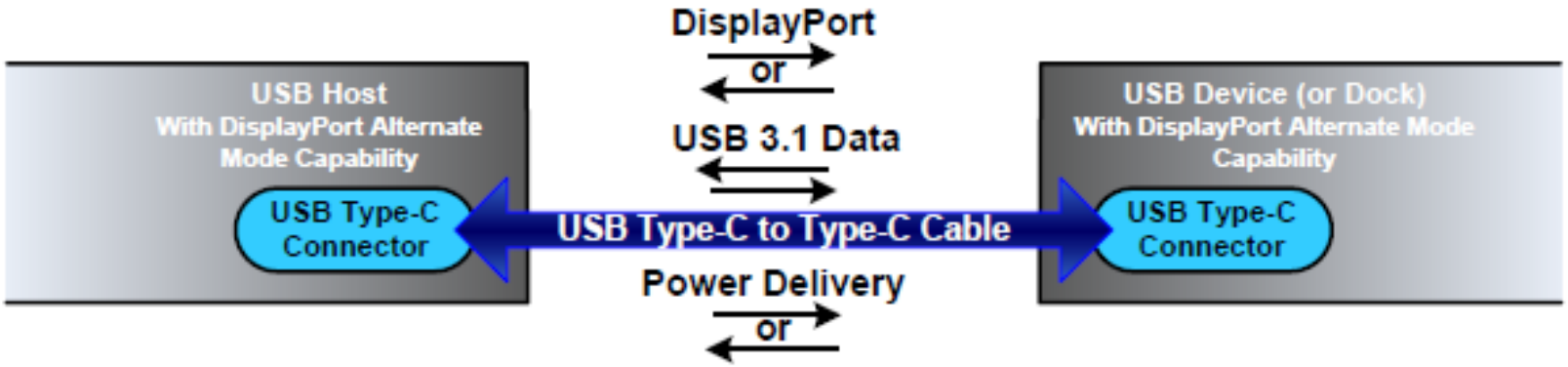
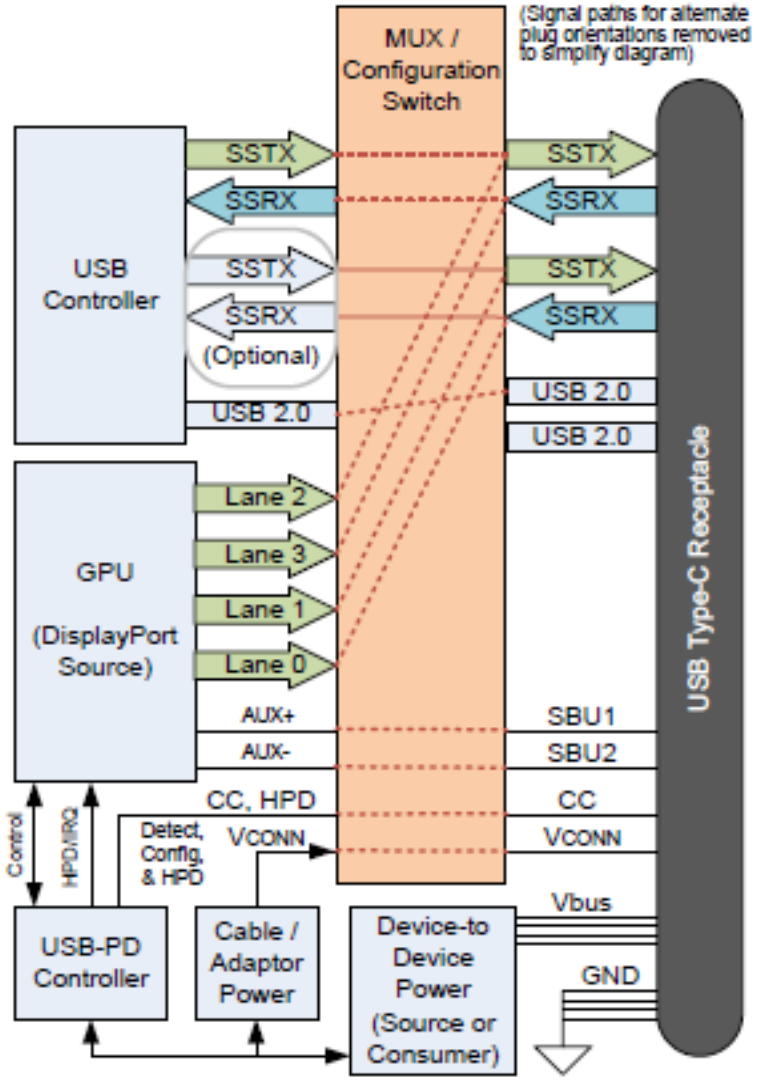
USB Type-C Connector Function Extension

DisplayPort Alternate Mode



- A passive Full Feature USB Type-C to Type-C cable can carry up to four DisplayPort lanes
  - This will offer the same performance and feature capability as a standard DisplayPort connection
  - This will also allow DisplayPort data rates to increase in the future, since the USB Type-C connector has very high data rate capability
- DisplayPort can be combined with USB 3.1 operation over the same USB Type-C cable
  - Implemented with two high speed pairs for DP (using two lane DP operation), and two high speed pairs for USB (USB 3.1 only uses two high speed lanes for normal operation)
  - Useful for docking stations or hubs, or for adding docking station functionality to a display
- USB 2.0 and USB Power Delivery is available in all configurations
  - Because USB 2.0 and USB Power Delivery use dedicated wires in the USB Type-C cable, both of these services are always available, even when using all four USB Type-C high speed pairs for DisplayPort

USB Type-C Connector PHY Switch for Supporting DisplayPort Alternate Mode



- Example for interface that supports USB and DisplayPort Alternate Mode
- Similar switch needed at the Device end
- Switch can be integrated along with the USB and DisplayPort functions

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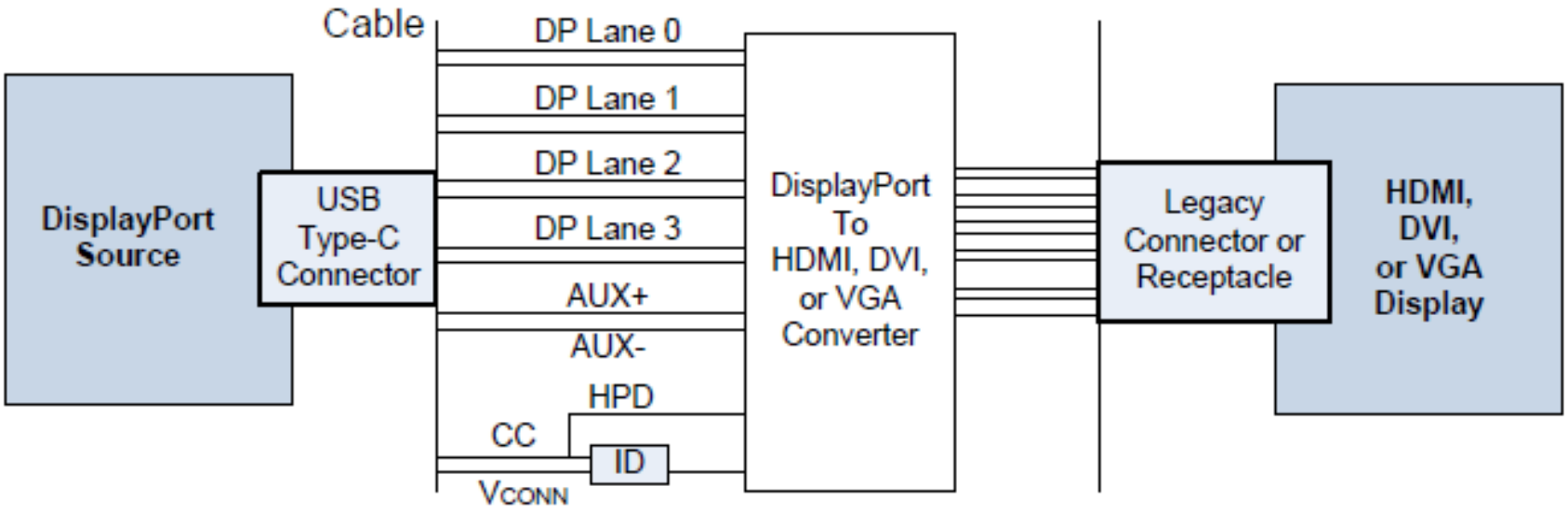
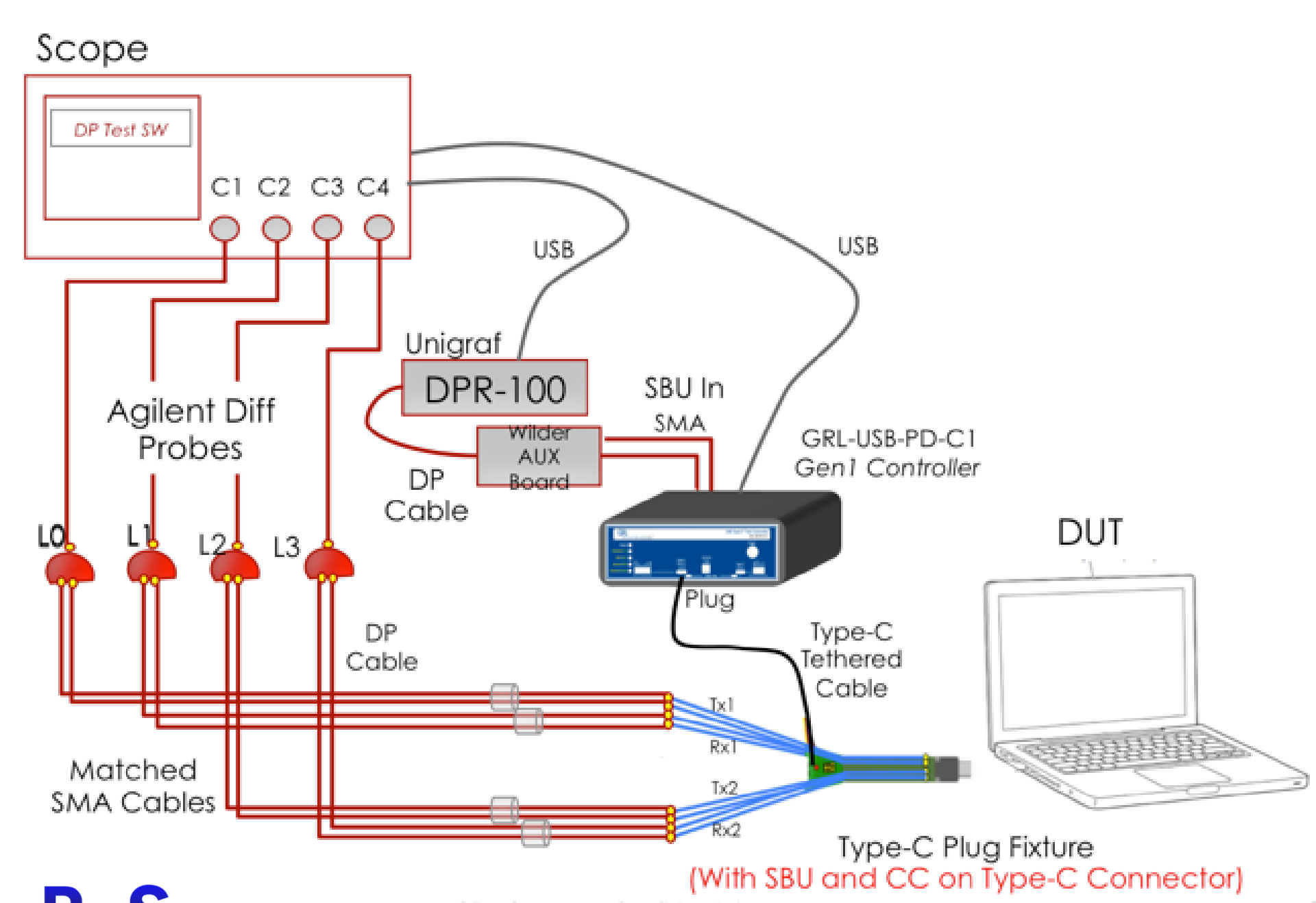
VESA DisplayPort

USB Type-C to HDMI, DVI and VGA Adapter Cables / Cable Adapters



- Utilizes DisplayPort Alt Mode capability of USB Type-C connector
- Adapter Cable: USB Type-C plug on one end, legacy plug on other end
- Adapter: USB Type-C plug on one end, legacy receptacle on other end
- USB Type-C will NOT support DisplayPort Dual Mode (DP++)
- USB Type-C to HDMI Converters will support HDMI 2.0 and CEC



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DPC Host test plan (Best Effort)

1. USB Type C test items
   a. USB PD tests => BMC Phy, Protocol
      Customer shall provide USB-PD .txt file
   b. USB 3.0 => Electrical Tx / Rx , LFPS
      Customer shall enable USB 3.0 PHY Compliance Test Patterns
   c. USB 2.0 => Electrical
   d. USB link layer tests
   e. USB 3.0 Gold tree Interop Tests

2. Displayport over USB Type C test items
   a. DPC source PHY test => main link , AUX eye
   b. DPC source Link layer Testing
   c. DPC Interop Testing
   d. DPC MST test if support
      Customer shall provide DisplayPort PHY (CDF)
      Customer shall provide tools for PHY Settings (Pattern, Level, Pre-Emphasis)

DPC Adapter test plan (Best Effort)

1. USB Type C test items
   a. USB PD tests => BMC Phy, Protocol
      Customer shall provide USB-PD .txt file
   b. USB 3.0 => Electrical Tx / Rx , LFPS if support USB 3.0
      Customer shall enable USB 3.0 PHY Compliance Test Patterns
   c. USB 3.0 Gold tree Interop Tests if support 3.0
   d. USB CV tests if support 3.0

2. Displayport over USB Type C test items
   a. DPC sink PHY test => main link , AUX eye
   b. DPC sink Link layer Testing
   c. DPC Interop Testing
      Customer shall provide DisplayPort PHY (CDF)
      Customer shall provide tools for PHY Settings
      (Pattern, Level, Pre-Emphasis)

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Example A

SuperSpeed USB Trident Logo
+ DisplayPort Logo

SuperSpeed USB Power Delivery Trident Logo
+ DisplayPort Logo

SuperSpeed USB 10 Gbps Power Delivery Trident Logo
+ DisplayPort Logo

Example B

SuperSpeed USB Trident Logo + MHL Logo

SuperSpeed USB Trident Logo + MHL Logo Symbol

SuperSpeed USB Power Delivery Trident Logo + MHL Logo

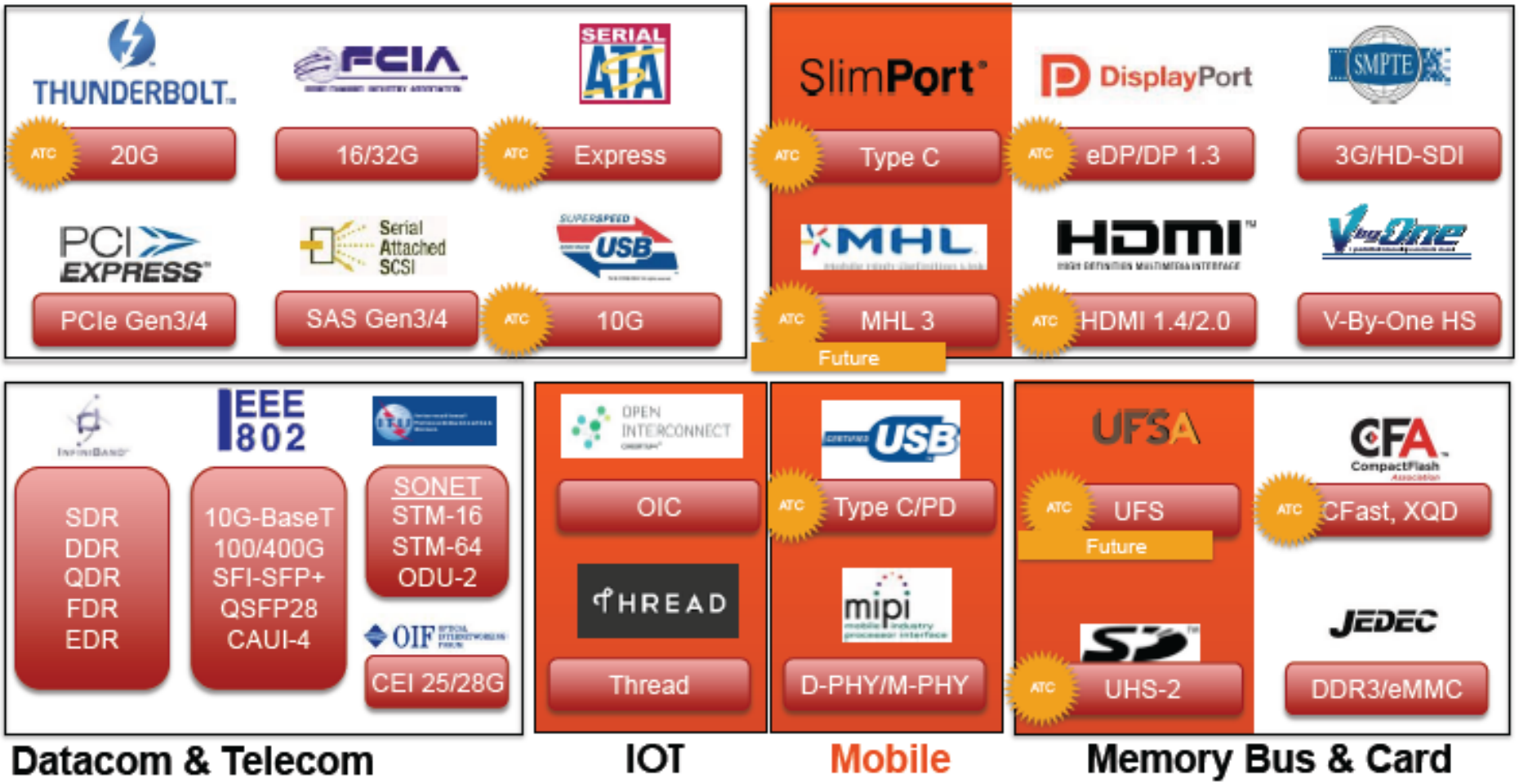
SuperSpeed USB Power Delivery Trident Logo + MHL Logo Symbol

SuperSpeed USB 10 Gbps Power Delivery Trident Logo + MHL Logo

SuperSpeed USB 10 Gbps Power Delivery Trident Logo + MHL Logo Symbol

Connectivity Standards Covered

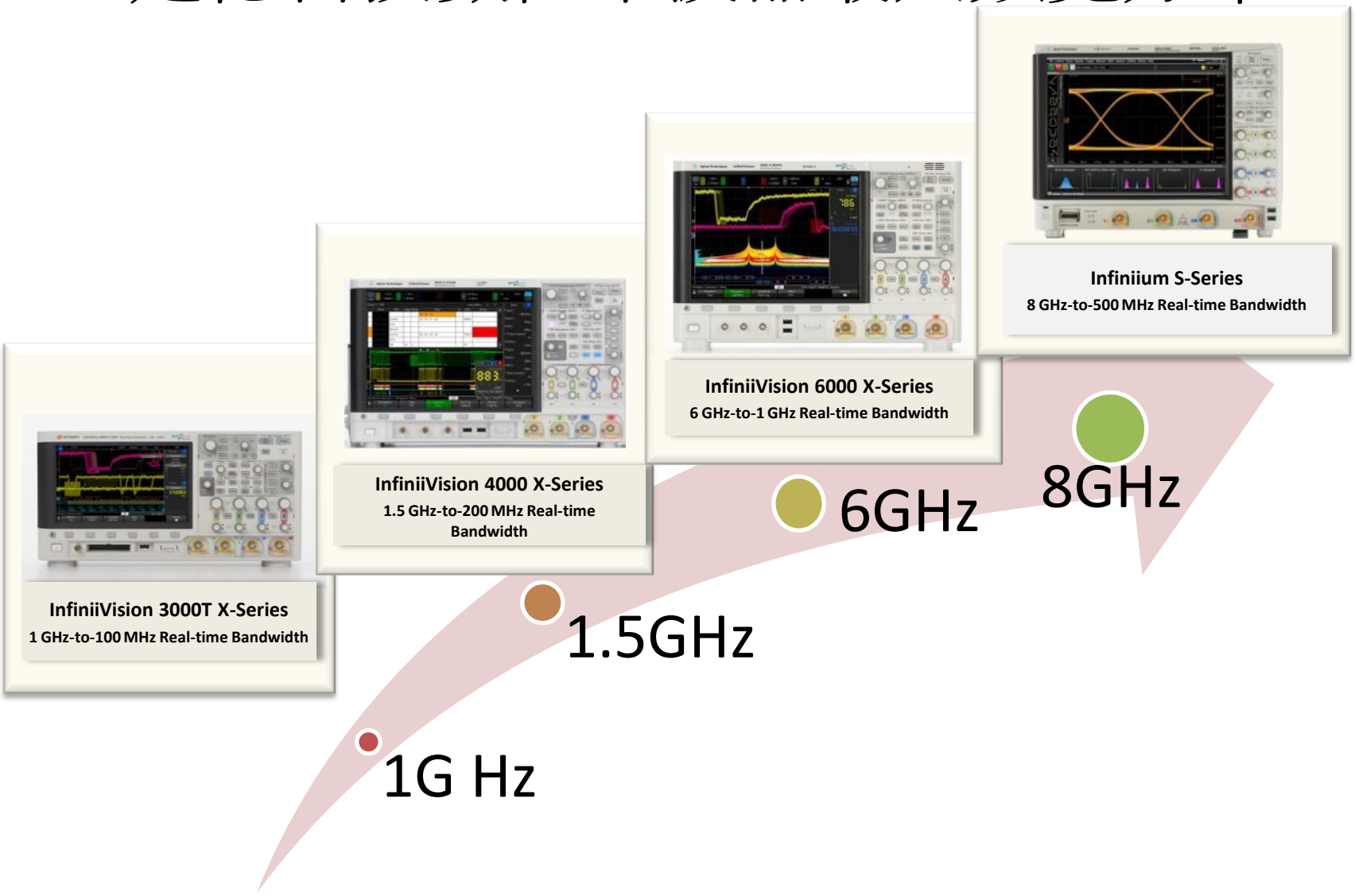
ATC Authorized Test Lab



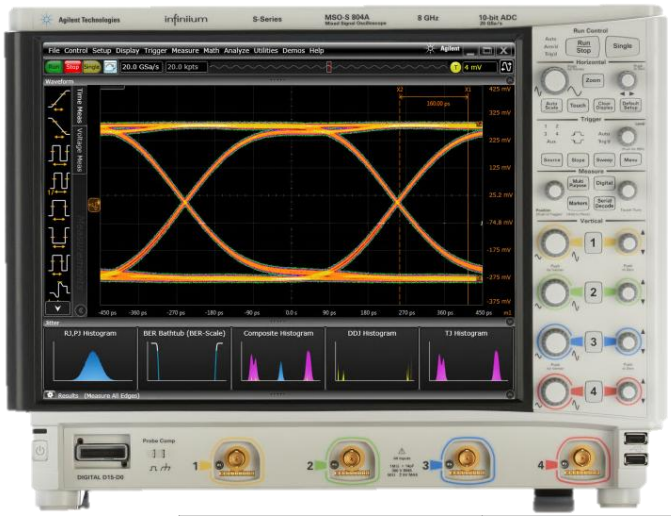
Keysight 產品介紹

品勛科技有限公司

是德科技數位示波器最大頻寬分布



Infiniium S-Series



- *500 MHz to 8 GHz DSO/MSO*
- *World's only **10 bit acquisition to 8 GHz***
- *New powerful, flexible interface with 15" capacitive multi-touch screen*
- ***Upgrade*** from a lower BW to a higher BW model at any time.

DSO Models	MSO Models	Analog Bandwidth 50 Ω input	Max Sample Rate	ADC bits	Standard Memory Depth
DSOS054A	MSOS054A	500 MHz	20 Gsa/s (2-ch) 10 GSa/s (4-ch)	10	100 Mpts (2-ch) 50 Mpts (4-ch)
DSOS104A	MSOS104A	1 GHz			
DSOS204A	MSOS204A	2 GHz			
DSOS254A	MSOS254A	2.5 GHz			
DSOS404A	MSOS404A	4 GHz			
DSOS604A*	MSOS604A*	6 GHz			
DSOS804A*	MSOS804A*	8 GHz			

Keysight Infiniium S-Series

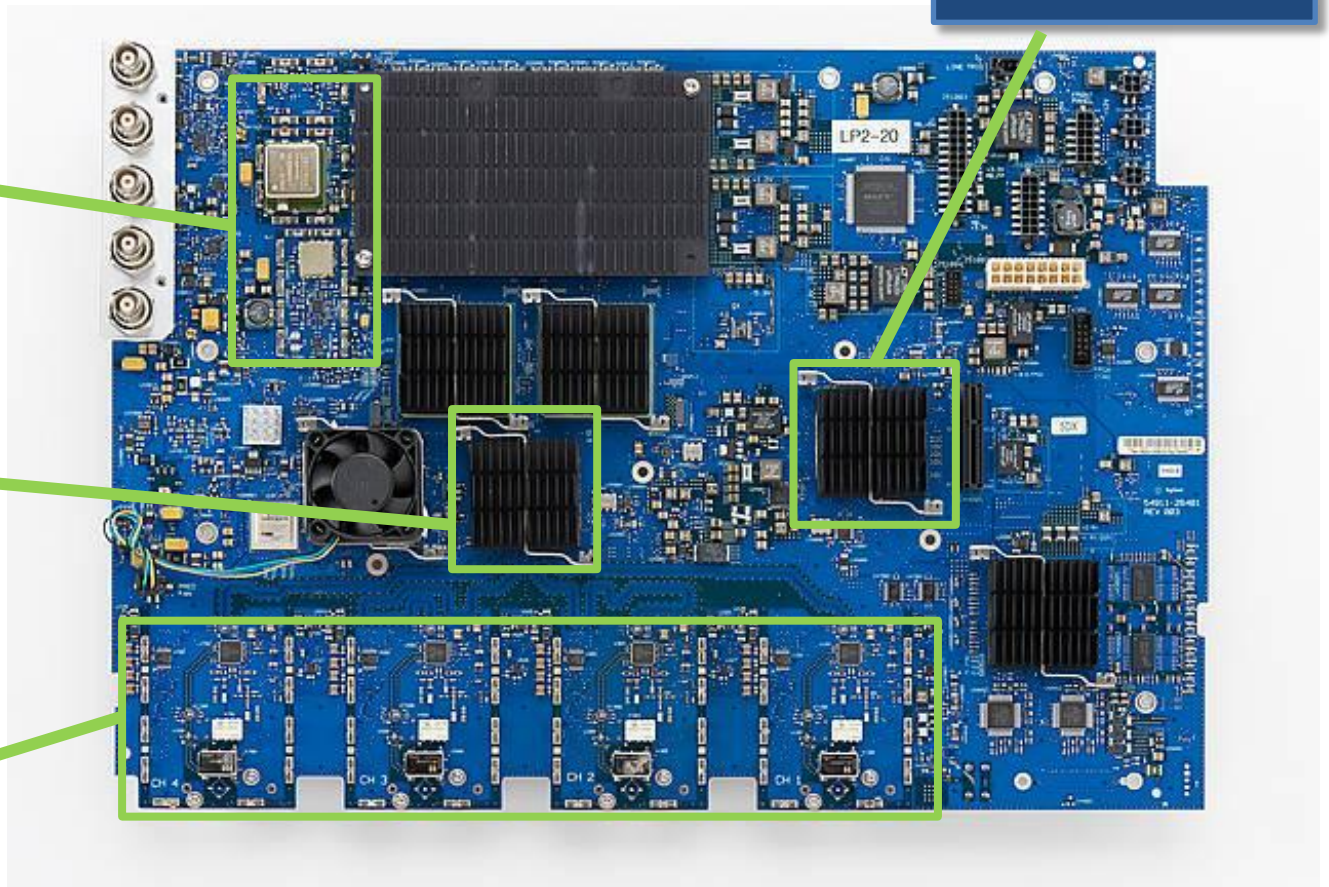
Hardware Innovation

Correction Filter FPGA

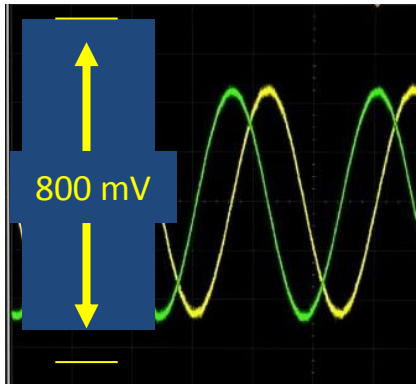
12 ppb accuracy timebase

New 10 bit, 40 GSa/s ADC

New low-noise front-end



ADC 解析度差異性



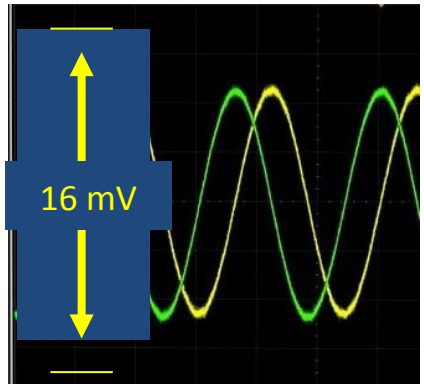
Traditional Scope
- 8 bits of vertical resolution
- 2^8 = 256 Q levels

3.125 mV

S Series ADC
- 10 bits of vertical resolution
- 2^{10} =1024 Q levels

0.781 mV

Minimum resolution
@ 800 mV full screen



Traditional Scope
- 8 bits of vertical resolution
- SW magnification at < 56 mV

218 uV*

S Series ADC
- 10 bits of vertical resolution
- 2^{10} =1024 Q levels

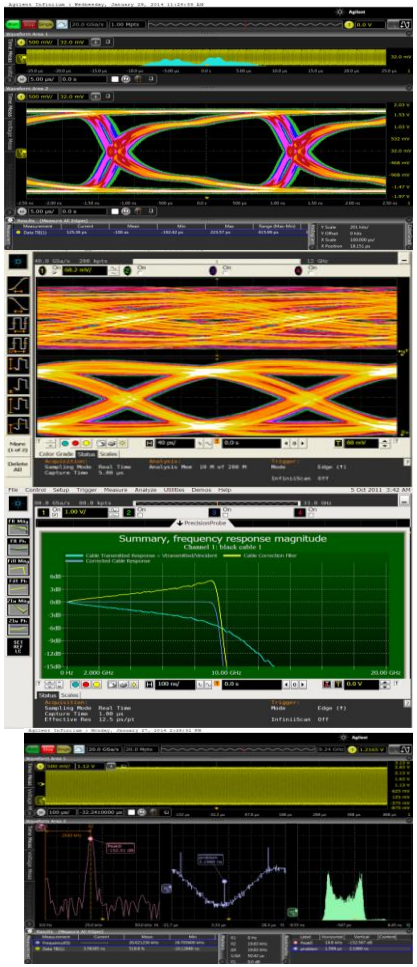
16.6 uV

Minimum resolution
@ 16 mV full screen

Infiniium S-Series測試軟體

Protocol Options

- 8B/10B
- CAN and CAN .dbc
- DigRF v4
- DVI
- HDMI
- FlexRay
- I2C/SPI
- JESD204B (contact factory)
- JTAG LIN
- MIPI CSI-3 (M-PHY)
- MIPI D-PHY MIPI LLI
- MIPI RFFE
- MIPI UniPro
- PCI e Gen1 and Gen2
- RS-232/UART
- SATA/SAS
- SPI
- SVID
- USB 2.0
- USB 3.0
- USB 3.0 SuperSpeed Inter-Chip (SSIC



Analysis Options

- DSA (EZJIT complete + SDA)
- Equalization
- EZJIt
- EZJIT+
- EZJIT Complete vertical noise analysis
- FPGA Dynamic Probe for Xilinx FPGAs
- InfiniiScan
- Infiniisim Basic
- InfiniiSim Advanced
- Matlab integration
- OSA (Oscilloscope Signal Analyzer)
- Power
- Precision Probe
- Serial Data Analysis
- UDA (User-defined application)
- UDF (User-Defined Function)
- VSA (Vector Signal Analysis)

Keysight N7020A Power Rail Probe

•低雜訊： 探棒採用 1:1 衰減比，可使示波器的基本雜訊僅增加 10%

•寬廣的偏移範圍： +/-24 V 的寬廣偏移範圍，方便使用者使用示波器最大的靈敏度設定，並將信號置於螢幕中心顯示

•低直流負載： 50 kΩ 直流輸入阻抗，大幅減少電源軌所增加的直流負載

•寬泛的主動信號範圍： 除偏移範圍外，主動信號範圍高達 +/-850 mV，方便使用者量測直流電源的快速暫態

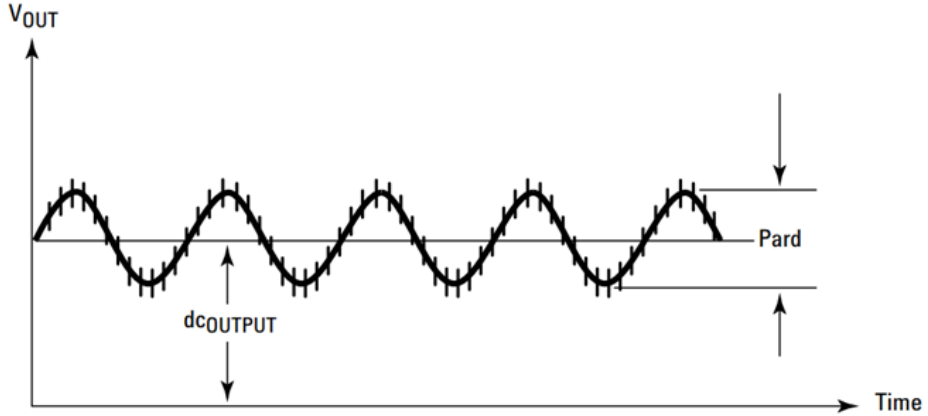
•高頻寬： 2 GHz 頻寬，可用於查找造成時脈和數位資料失真的快速暫態

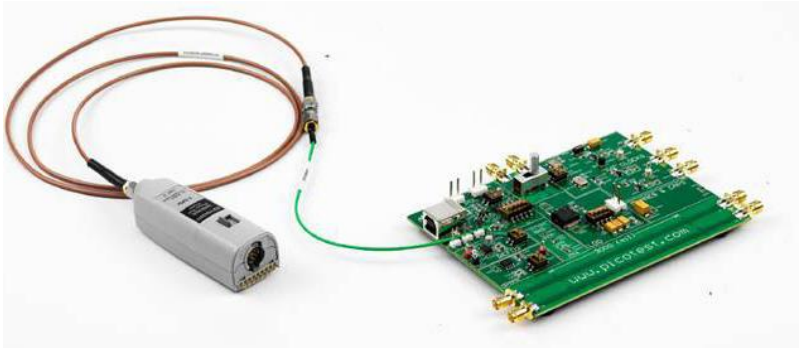
Keysight N7020A Power Rail Probe 應用

N7020A 電源探棒專爲電源完整性量測而設計，具有 mV 級靈敏度，可讓使用者更精確地探測直流電源上的雜訊、漣波和暫態。

該探棒非常適合量測隨機和週期干擾（PARD）、靜態和動態負載響應、可程式控制電源響應以及類似的電源完整性量測。

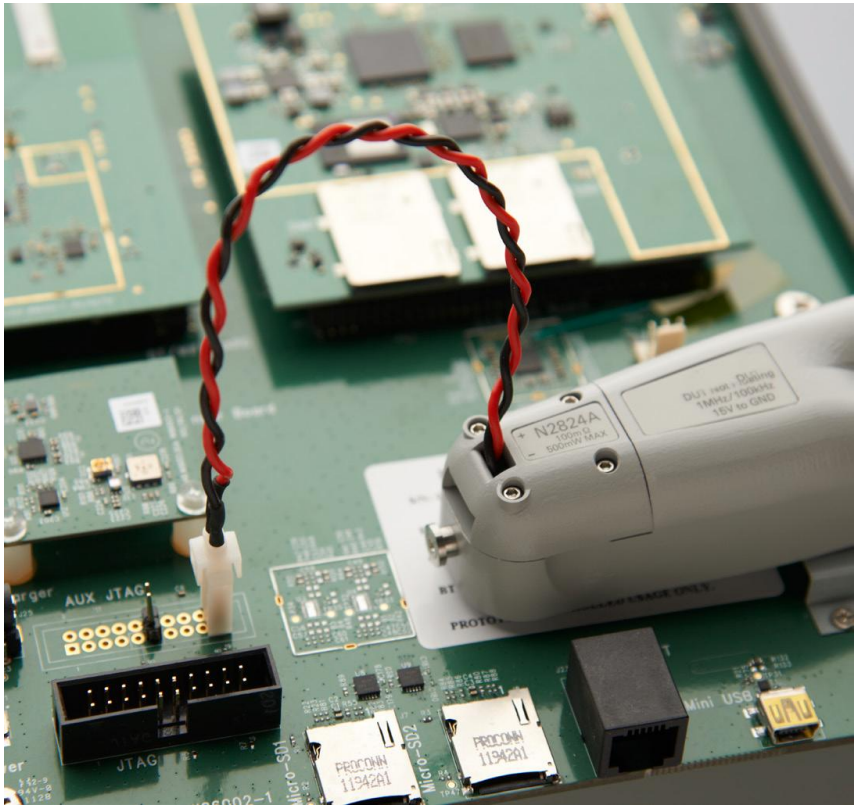
目前，大多數直流電源產品的容忍度要求變得非常嚴苛，N7020A 電源探棒可協助使用者確保他們設計的產品能夠滿足嚴格的容忍度要求。





Keysight N2820/21A

High-Sensitivity, High Dynamic Range Current Probes

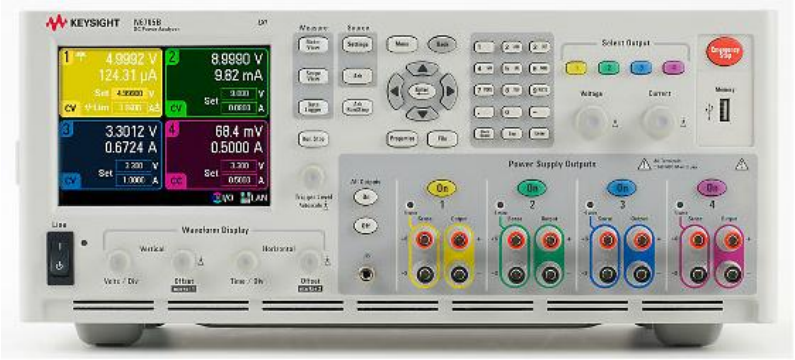


- 最小 50 uA的電流範圍
- 最大5 A的電流範圍
- >20,000:1或86 dB的寬動態範圍
- 頻寬: 3 MHz – 縮小通道

  500 kHz – 放大通道

Keysight N6705B DC Power Analyzer

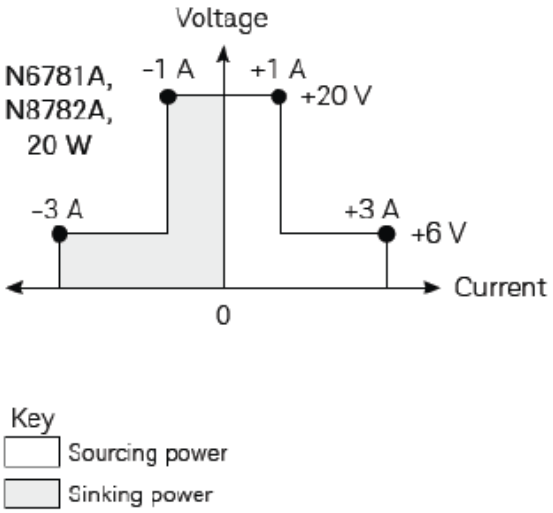
N6705B 不只是電源供應器，更是多功能電源分析儀

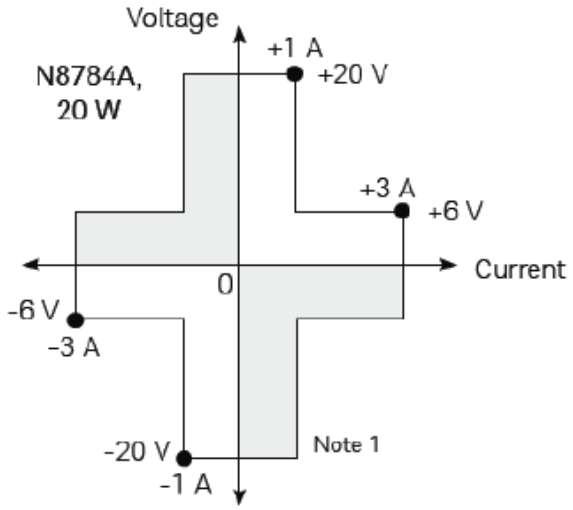


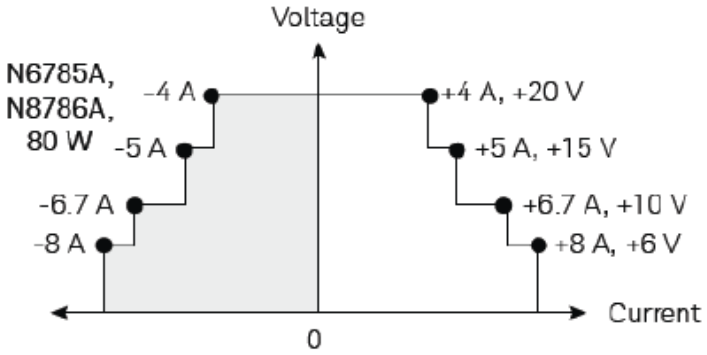
- 多通道電源供應器
- 任意波產生器
- 示波器
- 資料紀錄器
- SMU 無縫量程

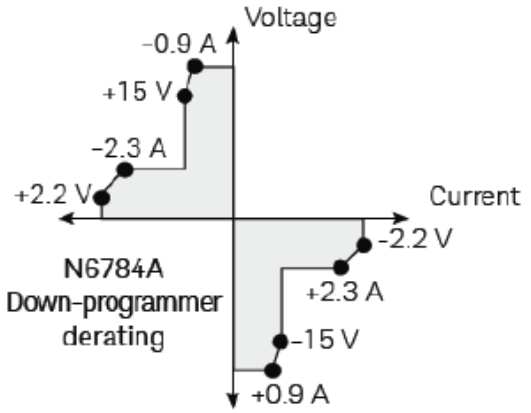
Keysight 14585A

N6705B SMU模組









手持式儀表免費延長兩年保固

- 適用機型：U5855A, U5856A, U5857A, U1451A, U1452A, U1452AT, U1453A, U1461A.
- 活動時間:至2016年5月31日

按讚回饋表單即可獲得
精美禮品喔!

詳情請至品勛科技官網查看